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TP7340F

SENSEUR DE VÉHICULES

DOSSIER CRIQ 632-4417

RAPPORT TECHNIQUE ELC-86-017

MAI 1986

F.C. 4623

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Montréal, le 29 mai 1986

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CENTRE DE RECHERCHE
INDUSTRIELLE DU QUÉBEC

TP7340F

SENSEUR DE VÉHICULES

PRÉPARÉ POUR LE:

CENTRE DE DÉVELOPPEMENT DES
TRANSPORTS, TRANSPORTS CANADA

PAR:

LE CENTRE DE RECHERCHE
INDUSTRIELLE DU QUÉBEC
C.R.I.Q.

Montréal, le 29 mai 1986

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INDUSTRIELLE DU QUÉBEC

Le contenu du présent rapport ne reflète que les opinions de l'auteur et ne saurait en aucun cas engager les politiques et positions officielles du Centre de développement des Transports, Transports Canada.

* An English summary of this report is included immediately preceding the table of contents.

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17. Résumé

De mars 1984 à avril 1986, des travaux de recherche ont été effectués au CRIQ. Ils avaient pour objet la conception et la construction de trois prototypes de senseur de véhicules à micro-ondes passifs utilisant comme capteur un radiomètre à micro-ondes, et un système digital moderne de traitement de l'information, d'emmagasinage et de transmission d'information.

Le projet de recherche débuta par la conception et la construction des radiomètres et fut suivi d'essais préliminaires. Après ces essais, une phase de recherche et de conception d'algorithmes fut entreprise et suivie d'une phase de simulation sur ordinateur. Les algorithmes développés furent implantés et améliorés suite aux divers essais effectués sur la route.

Les résultats des travaux ont prouvé que cette technologie était très fiable pour détecter la présence de véhicule; le taux d'erreurs dans le comptage est de moins de 1%. Le projet a aussi permis de vérifier que l'information concernant la taille (longueur) et la vitesse des véhicules pouvaient aussi en être déduite avec une bonne précision. Le projet a aussi démontré que l'appareil avait la possibilité d'évaluer l'état de la route (sec, mouillé, glacé).

Ce projet a donc démontré que la présente technique était opérationnelle et offrait des caractéristiques et des possibilités énormes pour le domaine du contrôle de la circulation.

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17. Abstract

This report documents research conducted from March 1984 to April 1986 at the Centre de recherche industrielle du Québec to design and build three prototypes of a passive microwave vehicle detector. A microwave radiometer served as the sensing head, and modern data processing, storage and transmission equipment was used.

The research project began with the design and construction of radiometers, after which preliminary trials were conducted. The next step was to research and develop algorithms, followed by computer simulation. The algorithms were then applied and improved in the light of field tests.

Results showed that the technology was extremely reliable in detecting the presence of vehicles, with an error rate of less than one per cent in the vehicle count. Tests also proved that vehicle length and speed could be measured accurately, and that road conditions (dry, wet, icy) could be identified.

The successful demonstration of the vehicle sensor has shown that the technology is feasible, offers a range of features and has excellent potential for traffic control.

18. Key Words	19. Distribution Statement
Sensor; microwave; vehicle; classification; speed; length; statistics; road transport.	A limited number of copies available from Transportation Development Centre

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SOMMAIRE

Différents organismes gouvernementaux ont besoin d'information au sujet du nombre et du type de véhicules qui passent, par unité de temps, en un point donné, sur une autoroute. Des appareils tels que des senseurs pneumatiques et des boucles magnétiques sont largement utilisés à cette fin. Cependant, dans certains cas, les techniques conventionnelles ne donnent guère de résultats satisfaisants, et il faut faire appel à des moyens plus élaborés.

Au fur et à mesure de l'augmentation de l'encombrement dans les villes et du trafic sur les autoroutes, des systèmes simples de contrôle de la circulation, à boucle ouverte, comme les feux de circulation à cycles fixes, deviennent de plus en plus inadéquats, et il devient impérieux d'adapter les méthodes de contrôle aux conditions actuelles de la circulation. Cette tendance se fait sentir par l'accroissement du nombre de feux de circulation contrôlés par le flux des véhicules, par les feux réglés en séquences, par les systèmes de contrôle intégrés et contrôlés par ordinateur du trafic urbain, et par les affichages programmables que l'on peut maintenant trouver sur certaines autoroutes.

Comme dans n'importe quel système, aussitôt que l'on passe de la boucle ouverte au contrôle en boucle fermée, il est nécessaire d'utiliser des senseurs pour fournir à l'appareil de contrôle les informations sur l'état actuel du système. En ce qui concerne le contrôle de la circulation, cette fonction est normalement remplie par un nombre de différents traducteurs, essentiellement ceux classifiés plus bas (tableau I).

TABLEAU I

ÉTAT DES SENSEURS

FONCTION DU SYSTÈME	TRADUCTEUR	DÉSAVANTAGES
Contrôle des feux circulation	1. Boucle magnétique sous la surface de la route	a) Coût d'installation élevé b) Implique des dommages pour le pavé c) Difficulté d'opération dans un environnement ferromagnétique
	2. Radar Doppler	a) Senseur actif (nécessite un permis) b) Ne peut déceler la présence d'un véhicule immobile c) Les reflets peuvent causer des interférences
Comptage des véhicules (autoroutes)	1. Comptage manuel	Très coûteux
	2. Senseurs pneumatiques	Endommagé facilement: inutilisable en hiver dans les pays nordiques
	3. Boucle magnétique	Installation coûteuse pour utilisation ponctuelle
Détection de la vitesse	1. Radar Doppler	a) Senseur actif b) Signaux des véhicules adjacents
	2. Senseurs pneumatiques	a) Visibilité pouvant affecter les habitudes de conduite b) Endommagé facilement

En plus des désavantages particuliers énumérés ci-dessus, on peut ajouter qu'aucune de ces techniques n'est appropriée en ce qui concerne la classification des véhicules selon leur catégorie.

Le présent projet englobait la conception et la construction d'un certain nombre de prototypes de senseurs de véhicules à micro-ondes passifs capables de percevoir la présence d'un véhicule, indépendamment de la vitesse, de classifier les véhicules qui passent selon leur catégorie, et de fournir, si nécessaire, d'autres données telles que l'état de la chaussée.

Les prototypes de senseur de véhicules utilisent comme capteur un radiomètre à micro-ondes et un système digital moderne de traitement de l'information, d'emmagasinage et de transmission d'information.

Le projet débuta par la conception et la réalisation d'un radiomètre "Dicke" portatif, opérant à 10,025 GHz et propre à un usage extérieur. Des essais ont été réalisés en utilisant cet instrument pour la détection des véhicules dans le trafic urbain et dans celui des autoroutes. Le radiomètre a fait ses preuves, avec succès, en donnant une indication claire du passage des véhicules. Lors de la phase d'analyse des résultats obtenus, il apparût que le senseur pouvait donner la mesure de la vitesse du véhicule, de sa longueur ainsi que l'état de la surface de la route (sec, mouillé ou glacé). Cependant, étant donné la grande variété de véhicules (diverses formes), la mise au point des algorithmes pouvant extraire ces informations fût très ardue et élaborée.

En regard des désavantages des différentes techniques établies (tableau I), le projet a démontré que le senseur de véhicules à micro-ondes présentait des aspects très intéressants. Le tableau qui suit (tableau II) résume les caractéristiques techniques et opérationnelles de l'appareil.

Les résultats des essais ont démontré que cette technologie était très fiable pour compter les véhicules; le taux d'erreurs dans le comptage est de moins de 1%. Les résultats ont aussi permis de vérifier que la vitesse et la longueur des véhicules pouvaient être déduites avec une bonne précision.

Ce projet a donc démontré que la présente technologie était opérationnelle et offrait des caractéristiques et des possibilités énormes pour le domaine du contrôle de la circulation.

TABLEAU II

DÉTECTEUR DE VÉHICULES A MICRO-ONDES
Caractéristiques du prototype

. COMPTAGE DES VÉHICULES
. INDICATION DE LA VITESSE ET DE LA LONGUEUR DES VÉHICULES
. INSTALLATION PERMANENTE OU TEMPORAIRE
. UTILISATION DANS TOUTES LES CONDITIONS CLIMATIQUES
. OPÉRATION DANS UNE VOIE UNIQUE
. SEUIL MULTI-NIVEAUX
  TAILLE DES VÉHICULES
  PLAGE DES VITESSES
. TRANSMISSION DE L'INFORMATION A UN ORDINATEUR (SUR DEMANDE) ET A UN PÉRIPHÉRIQUE
. NE NÉCESSITE AUCUNE MODIFICATION DE LA CHAUSSÉE
. MONTAGE DIRECTEMENT AU-DESSUS DE LA ROUTE OU EN POSITION ÉLEVÉE SUR LES COTÉS
. SENSEUR A DISTANCE COMPLÈTEMENT PASSIF (QUI N'ÉMET AUCUN SIGNAL)
. LÉGER-ROBUSTE
. INDICATION DE L'ÉTAT DE LA ROUTE (SEC, MOUILLÉ OU GLACÉ)
. INDICATION DE L'HEURE, DE LA VITESSE ET DE LA TAILLE LORS DE LA DÉTECTION D'UN VÉHICULE

SUMMARY

Many government agencies require information on the number and type of vehicles passing a given point within a given time. Such information is currently collected by such devices as pneumatic sensors and magnetic induction loops. In some cases, however, conventional methods do not yield satisfactory results, and more sophisticated techniques are necessary.

As congestion in cities grows and traffic density on highways increases, simple "open loop" systems of traffic control - fixed-cycle traffic lights, for example - become more and more unsatisfactory. Control procedures have therefore had to be adapted to traffic conditions, as evidenced by the growing number of vehicle-controlled traffic lights, phased-sequence traffic of lights, integrated computer-controlled systems, and programmable displays that have been installed on freeways.

As in any system, switching from open to closed loop control means that sensors are needed to provide the controller with information on the current status of the system. In traffic control, this function is usually performed by a number of different transducers, primarily those listed in Table I.

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TABLE 1

FUNCTION	TRANSDUCER	DISADVANTAGES
Traffic light control	1) Inductive loop under road	a) Expensive to install b) Possible damage to pavement c) Difficulty to operate in ferromagnetic environment
	2) Doppler radar	a) Active sensor (requires licence) b) Cannot detect stationary vehicles c) "Glint" can cause confusing signals
Vehicle counting (highways)	1) Manual counting	Very expensive
	2) Pneumatic tubes	Easily damaged; unusable in northern climates in winter
	3) Inductive loops	Expensive installation for occasional use
Speed detection	1) Doppler radar	a) Active sensor b) Signals from adjacent vehicles
	2) Pneumatic tubes	a) Visibility may change driving patterns b) Easily damaged

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In addition to their specific disadvantages, none of the methods listed in the table is suitable for classifying vehicles by type.

The purpose of this project was to design and build prototypes of passive microwave sensors that could detect the presence of a vehicle whatever its speed, classify it, and provide other data, such as information on road conditions, if necessary.

A microwave radiometer served as the sensing head, and modern data processing storage and transmission equipment was used.

The first step was to design and build a portable "Dicke" radiometer for outdoor use. The radiometer, operating at 10.025 GHz, was tested for its ability to detect vehicles in city and highway traffic. The instrument was a success, clearly indicating passing vehicles. Test results also showed that the sensor could measure vehicle speed and length and identify road conditions (dry, wet or icy). Because of widely varying vehicle configurations, however, designing suitable algorithms proved very difficult.

The project showed that the microwave sensor, in contrast with the methods listed in Table I, offers some interesting features. Its technical and operating characteristics are summarized in Table II.

The results of trials proved the technology to be very reliable in detecting passing vehicles, with a vehicle count error rate of less than one per cent, and capable of providing accurate measurements of vehicle length and speed.

The successful demonstration of the microwave sensor proves that the technology is feasible, offers a range of features, and has excellent potential for traffic control.

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TABLE II

MICROWAVE VEHICLE SENSOR
Prototype features

- VEHICLE COUNT CAPABILITY
- VEHICLE SPEED AND LENGTH MEASUREMENT
- PERMANENT OR TEMPORARY INSTALLATION
- ALL-WEATHER OPERATION
- SINGLE-LANE OPERATION
- MULTI-LEVEL THRESHOLD
  SIZE OF VEHICLES
  RANGE OF SPEEDS
- TRANSMITS INFORMATION TO A COMPUTER (ON REQUEST) AND ONE PERIPHERAL
- NO ROAD WORK NECESSARY
- MAY BE INSTALLED HIGH ABOVE OR BESIDE THE ROAD
- WHOLLY PASSIVE REMOTE SENSOR (NO SIGNAL EMITTED)
- LIGHT AND STURDY
- IDENTIFIES ROAD CONDITIONS (DRY, WET OR ICY)
- INDICATES TIME AT WHICH VEHICLE PASSES, ITS SPEED AND LENGTH

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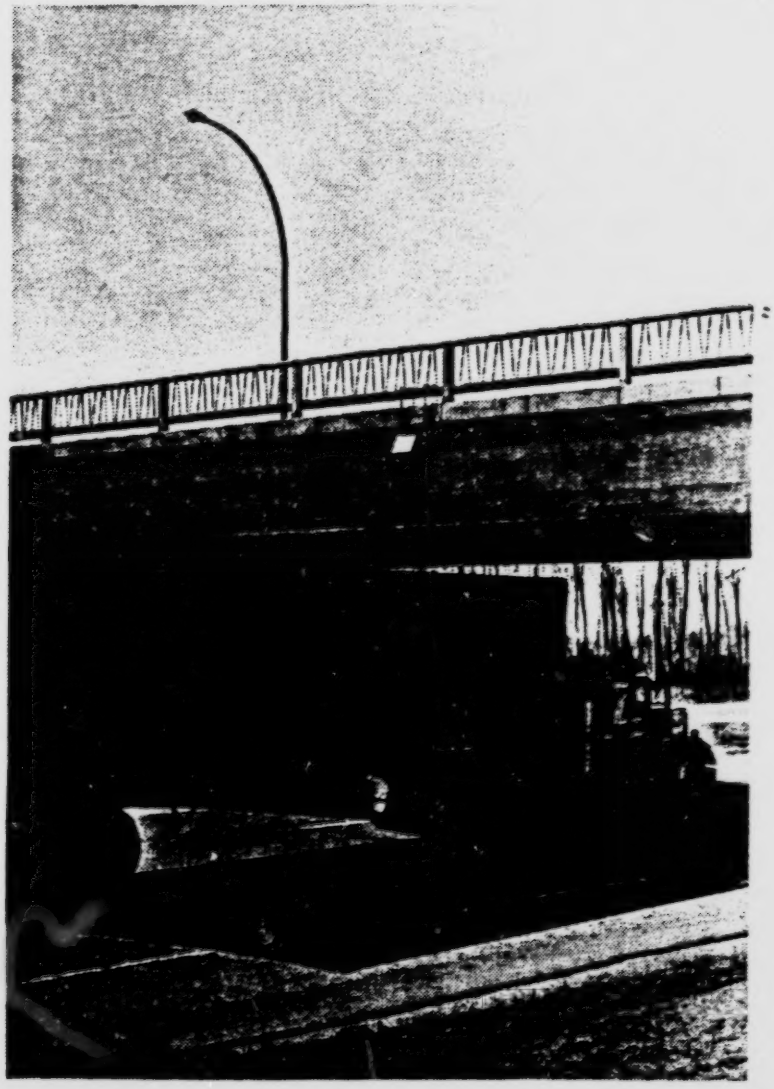
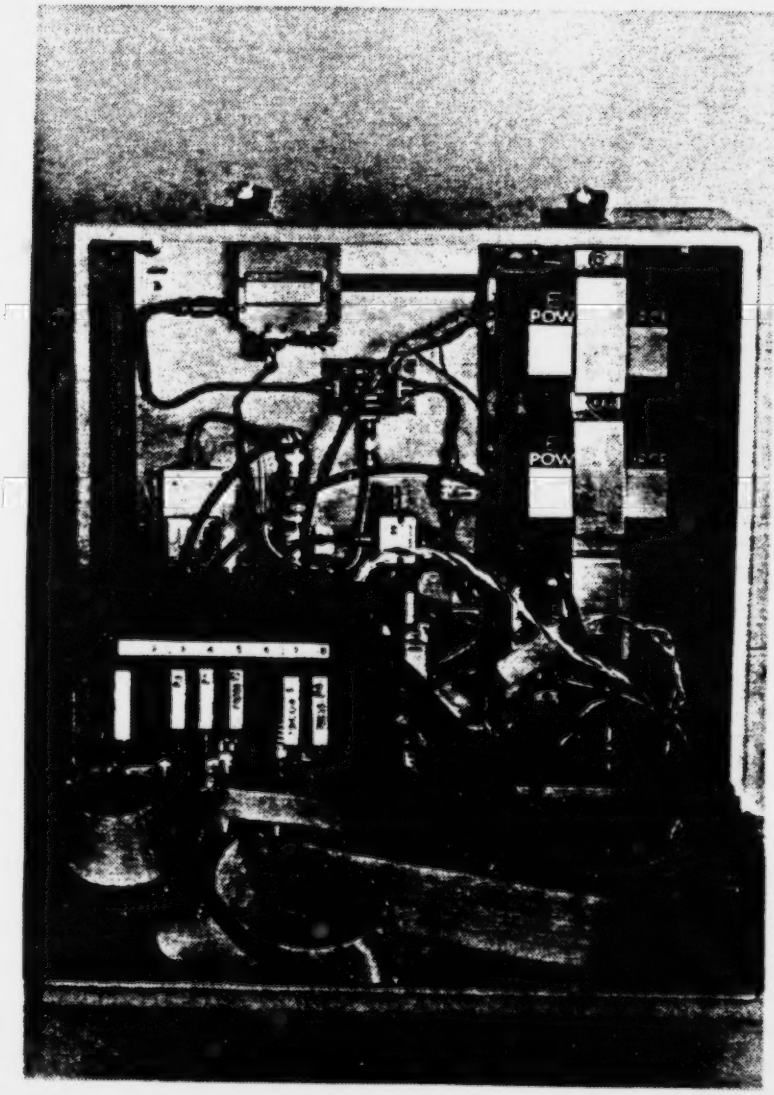


INSTALLATION TYPIQUE DU SENSEUR DE VÉHICULES



VUE INTÉRIEURE DU SENSEUR DE VÉHICULES

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APPENDICE I: Logiciel: Senseur de véhicules

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1 INTRODUCTION

Ce rapport technique décrit le système et le fonctionnement du détecteur de véhicules par micro-ondes. Il comprend les caractéristiques techniques et fonctionnelles de l'appareil ainsi qu'une description de chacune des fonctions.

Une description technique des circuits électroniques et du logiciel employés dans l'appareil se trouve à la section 4 du rapport.

La section 5 donne un sommaire des résultats ou performances obtenus, des conclusions du travail de recherches et des recommandations.

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2 DESCRIPTION TECHNIQUE DU SENSEUR DE VÉHICULES A MICRO-ONDES

2.1 Caractéristiques générales

2.1.1 Principe d'opération

Un radiomètre à micro-ondes réagit principalement à la portion micro-ondes du rayonnement émis par tous les objets dégageant de la chaleur. Lorsqu'il est utilisé comme senseur de véhicules et braqué vers le bas sur une route, le radiomètre effectuera, en l'absence de véhicule, la lecture de la température de la route (c'est-à-dire environ 300°K). Cependant, lorsqu'un véhicule passe, celui-ci réfléchit le rayonnement du ciel dans le radiomètre, et ce rayonnement est caractérisé par une température beaucoup plus basse (généralement aux environs de 10°K). Cette variation de la température apparente donne un changement perceptible dans les signaux de sortie du radiomètre.

2.1.2 Géométrie du faisceau

Le faisceau est suffisamment directionnel pour n'inclure dans le faisceau principal que les voies de circulation nécessaires et possède des faisceaux latéraux raisonnablement bas. Etant donné que l'on a besoin de la longueur du véhicule, la largeur du faisceau doit permettre d'englober tout le véhicule.

On suppose que l'instrument est placé à 24 pieds de hauteur et dirigé uniquement sur une voie, il est donc nécessaire d'avoir un faisceau d'environ 60° X 30°, de sorte que l'antenne dans la bande X soit plutôt petite (environ 3 cm X 9 cm).

2.1.3 Analyse de la forme d'ondes

Afin de démontrer qu'il est possible d'extraire des informations des véhicules passant dans le champ du radiomètre, l'analyse simple est présentée ci-dessous. Le champ de vision est schématisé comme un cône ayant un angle d'ouverture θ et une origine situés à une hauteur H de la route (voir figure 2).

Deux (2) cas devraient être examinés selon le ratio relatif des deux (2) longueurs équivalentes ℓ et L, qui sont respectivement la longueur équivalente d'un véhicule et

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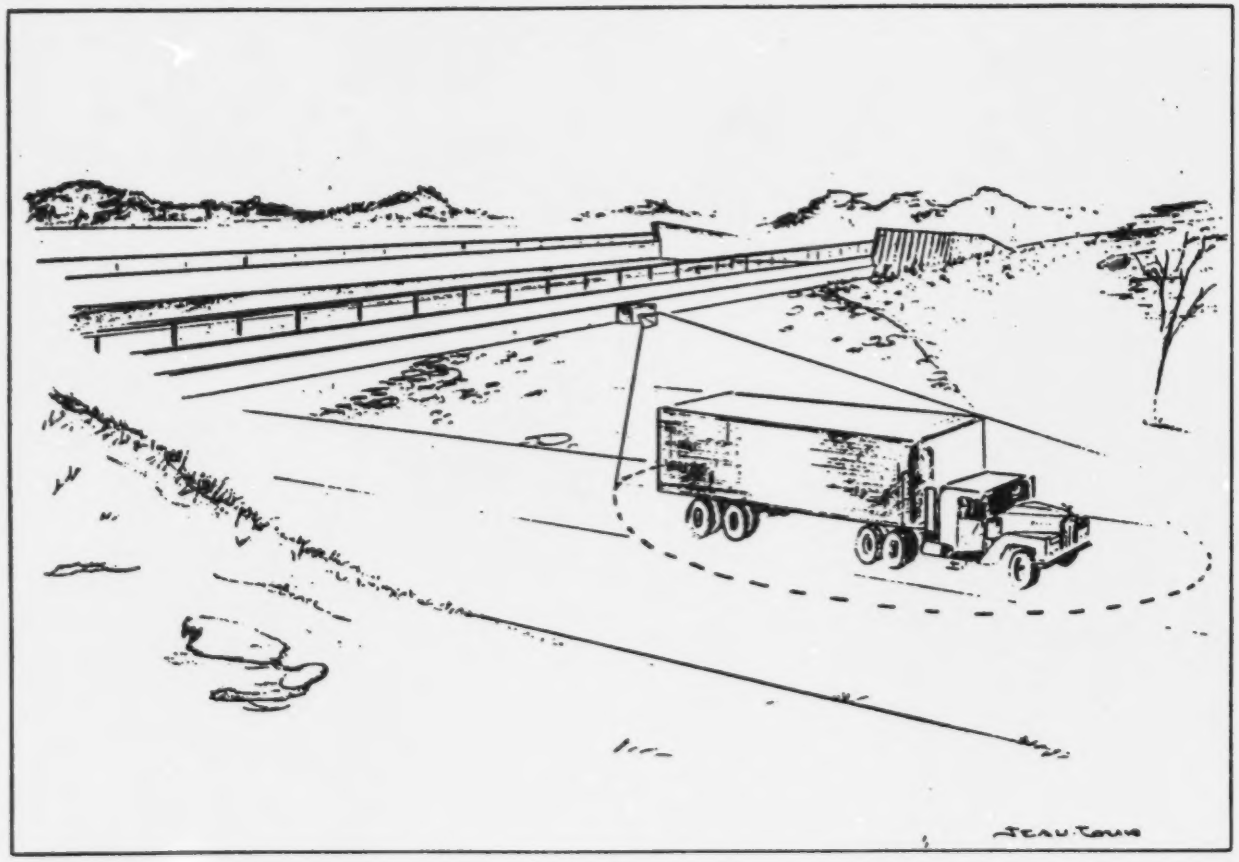

Fig. 1: Géométrie du faisceau

la surface sur le sol illuminé par le faisceau. On supposera ici, pour simplifier, que $L > \ell$. La figure 2 visualise le mouvement d'un véhicule qui passe dans le cône en différents temps consécutifs et numérotés.

La forme d'ondes simplifiées obtenue au signal de sortie du radiomètre se présente sous l'aspect illustré à la figure 3.

En supposant que la vitesse V du véhicule qui passe à travers le faisceau est constante, on peut déduire les équations suivantes:

$$Ta = \frac{L + \ell}{V}$$

$$Tb = \frac{L - \ell}{V}$$

$$Tc = \frac{\ell}{V}$$

L: Longueur équivalente du faisceau idéal près du sol
ℓ: Longueur équivalente d'un véhicule
V: Vitesse moyenne d'un véhicule

Les dérivations de V et sont comme suit:

$$V = \frac{2L}{Ta + Tb} = \frac{L}{Tb + Tc}$$

$$\ell = L \frac{Ta - Tb}{Ta + Tb}$$

On peut traiter les caractéristiques d'un véhicule (vitesse: V et longueur: ℓ) à partir des mesures de durée du temps et de la longueur L estimées.

Le changement d'apparence de ces formes d'ondes, alors que V et ℓ varient, est montré à la figure 4.

2.1.4 Conditions de la route

Le principe de la tête du radiomètre est de donner un signal de sortie qui varie avec la température perçue par l'antenne. En l'absence d'un véhicule, cette température ne dépend que des conditions de la route, ce qui affecte la quantité d'énergie captée par le faisceau. Des essais ont montré que les conditions de la route produisaient des changements mesurables dans le niveau de référence et dans le bruit de fond.

Par conséquent, il est suffisant de mesurer ces niveaux pour décider si la route est sèche, mouillée ou glacée.

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L • LONGUEUR EQUIVALENTE DU FAISCEAU PRES DU SOL

ℓ • LONGUEUR EQUIVALENTE D'UN VEHICULE

v • VITESSE MOYENNE D'UN VEHICULE

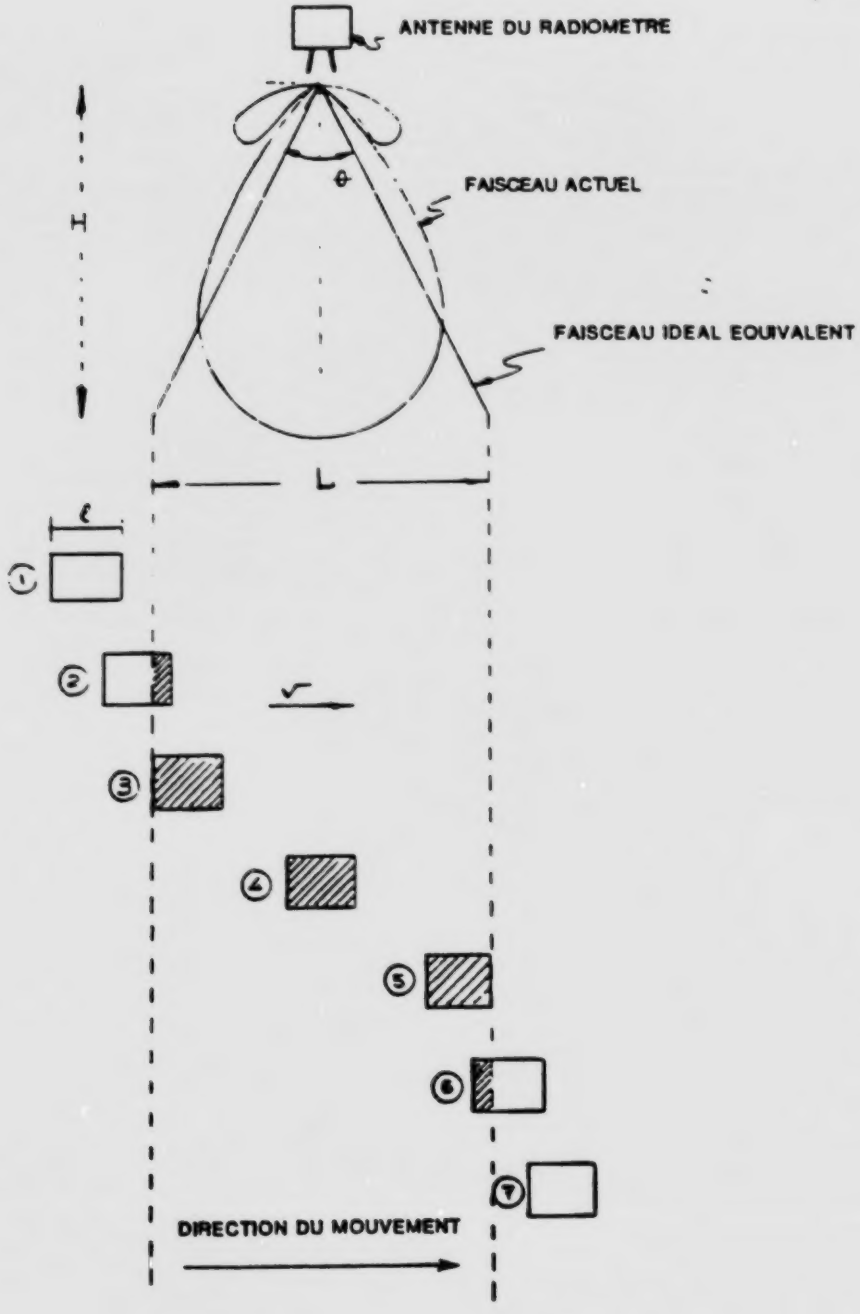

FIGURE 2 – PASSAGE D'UN VEHICULE A TRAVERS LE FAISCEAU

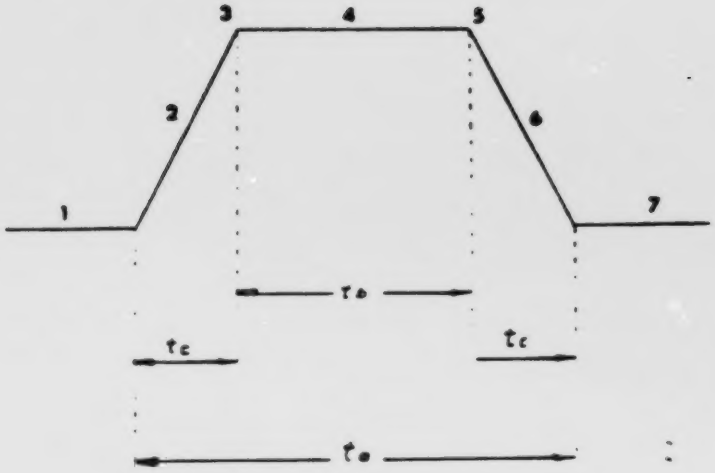

FIGURE 3 - SCHEMA DE LA FORME D'ONDE

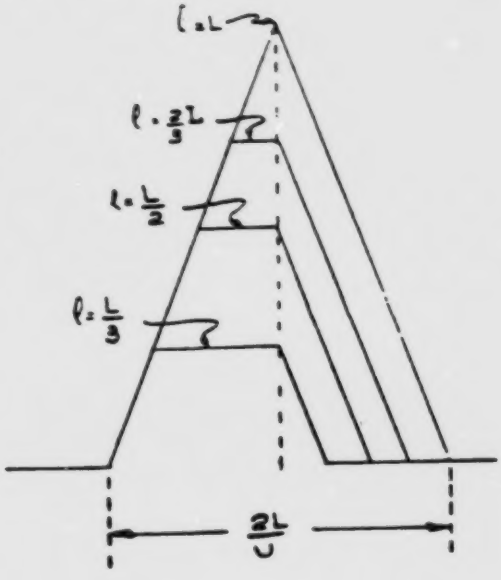

FIG. 4a VITESSE CONSTANTE
LONGUEURS VARIEES

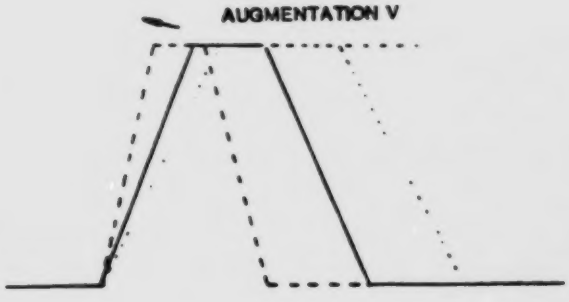

FIG. 4b LONGUEUR CONSTANTE
VITESSES VARIEES

FIGURE 4 - EFFETS DES PARAMETRES V ET ℓ SUR LA FORME D'ONDE

2.2 Schéma bloc

Cette section décrit les différents modules qui sont utilisés dans le dispositif. La figure 5 montre les principaux modules électroniques d'un tel système, au coeur duquel il y a un micro-contrôleur. Ce contrôleur a pour fonction principale la surveillance des différents sous-systèmes qui lui sont rattachés, et le traitement de l'information du senseur micro-ondes ou de la ligne de communication. Tout cela s'accomplit sous le contrôle de divers programmes permanents, emmagasinés dans la mémoire morte programmable (EPROM).

2.2.1 Le radiomètre

Le principe du radiomètre Dicke est utilisé ici. Il s'agit d'un comparateur de bruit à large bande fonctionnant dans la "bande X". La température du bruit d'antenne est comparée (utilisant un interrupteur et un détecteur synchrone) avec celle d'une charge de référence.

Quoique des soins considérables soient nécessaires lors de la construction d'un radiomètre de haute précision (mieux que +1°K), notre instrument n'a pas besoin d'être si sophistiqué.

Afin de supprimer le bruit près de la porteuse de la source, et le bruit de basse fréquence des diodes, on utilise une fréquence de coupure inférieure relativement élevée (10 MHz dans le prototype). Il est alors possible de calculer le facteur de bruit (pré-détection) requis à partir de l'équation:

$$T = \frac{\pi}{2} \frac{NF\ (To + Ta)}{\sqrt{B\tau}}$$

Lorsque To est la température de la tête
Ta est la température de la charge de l'antenne
T est la sensibilité à la température
B est la largeur de bande
τ est le temps d'intégration à la sortie
NF est le facteur de bruit (pré-détection)

Pour l'application présente, une sensibilité d'environ 10°K est suffisante, et avec un temps d'intégration de 0,01s, le facteur de bruit requis est d'environ 25. Etant donné les facteurs de bruit de 5 (typique) et 10 (maximum) d'un mélangeur moderne, ce facteur n'est pas difficile à obtenir.

CRIQ CENTRE DE RECHERCHE INDUSTRIELLE DU QUÉBEC

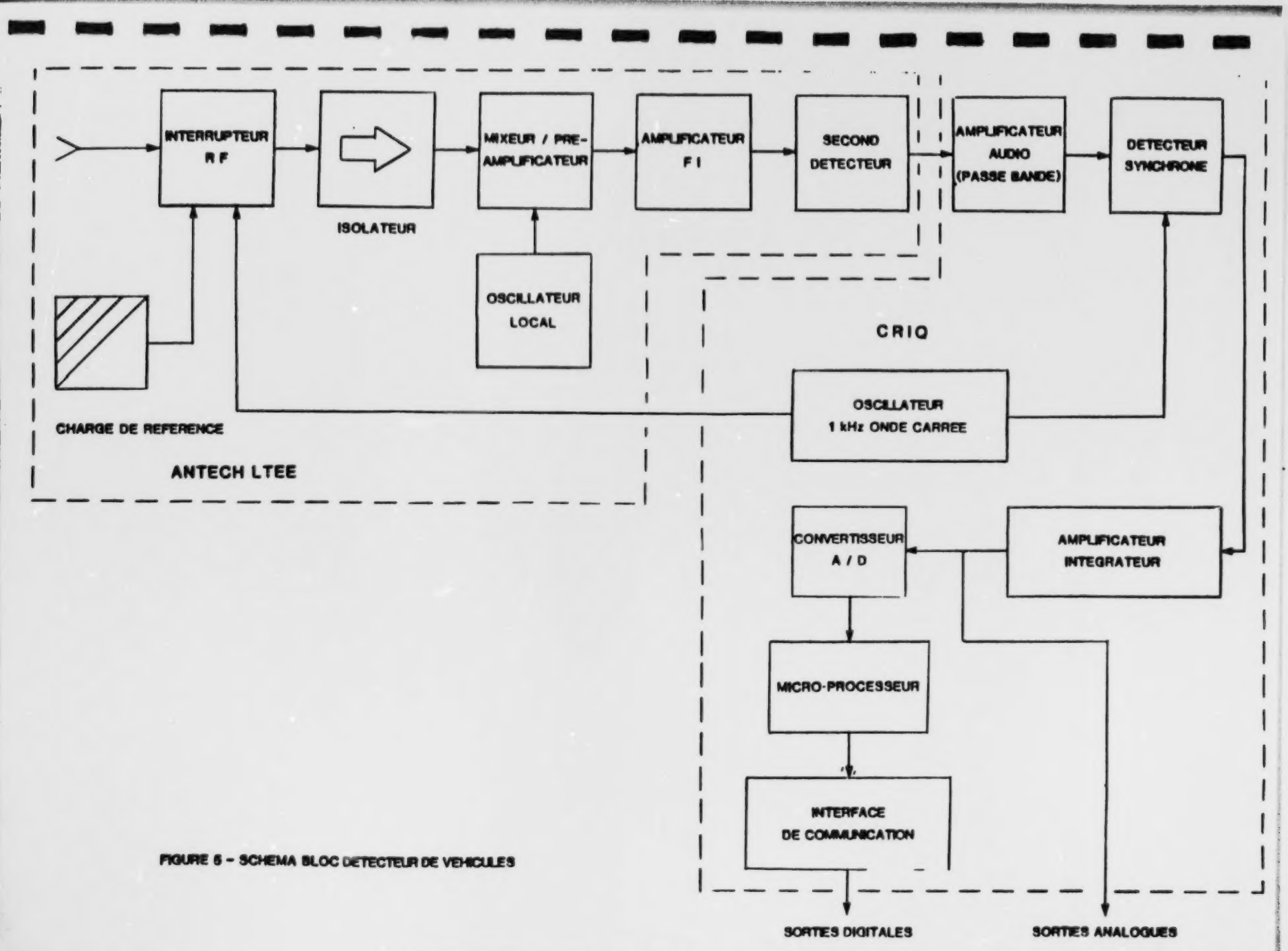

FIGURE 5 - SCHEMA BLOC DETECTEUR DE VEHICULES

Le signal à l'entrée du mélangeur est un bruit thermique d'une largeur de bande d'environ 1000 MHz provenant alternativement de l'antenne (température d'antenne) et de la charge adaptée (température de référence).

La composante alternative du signal de sortie du mélangeur est transmise au pré-amplificateur, lequel amplifie les deux (2) bandes latérales du bruit à large bande. Le signal est ensuite amplifié par un amplificateur de fréquence intermédiaire. Ce signal de fréquence intermédiaire d'une largeur de bande de 500 MHz est amplifié à un niveau adéquat pour une détection par un détecteur à diode ("point contact crystal detector"), suivi d'une amplification audio dans une bande de 10 Hz à 30 Hz. A ce point, le signal est une onde carrée bruitée, correspondant à la modulation d'onde carrée à l'entrée du mélangeur.

Les prototypes sont construits à l'aide de composants disponibles dans le commerce.

2.2.2 Pré-traitement du signal

Cette onde carrée est redressée dans le détecteur synchrone, lequel multiplie le signal avec celui de l'oscillateur utilisé pour l'opération de l'interrupteur R.F. Ce système de charge de référence et de détection aide à réduire le bruit causé par les variations à basse fréquence dans le gain de l'amplificateur. (En fait, tous les bruits dont la fréquence est 1 kHz).

Après la détection synchrone, le signal est filtré avec une constante de temps assez longue (0,01s) pour fournir un niveau proportionnel à la différence entre les températures d'antenne et de la charge de référence. Ce signal est amplifié à un niveau approprié pour la conversion analogue à digital, et pour une sortie analogue.

2.2.3 Module calculateur

Le processeur accepte le signal digital d'entrée et le traite afin d'obtenir les mesures de la taille et de la vitesse des véhicules qui passent, en tenant compte des facteurs comme la variation de la température ambiante. Le nombre de véhicules dans chaque catégorie de taille et de vitesse est emmagasiné dans la mémoire, cette dernière possède une capacité suffisante pour 24 heures de données.

La présente technologie permet une approche économique et très versatile utilisant les composants digitaux intégrés modernes, tels qu'un microprocesseur (CPU: Central Processing Unit), des mémoires volatiles (RAM: Random

CRIQ

Access Memory), des mémoires reprogrammable (EPROM: Erasable Programmable Read Only Memory), une interface de communication (UASRT: Universal Asynchronous Receiver Transmitter), des périphériques (I/O: Input/Output ports), un circuit convertisseur analogue à digital, et un circuit d'horloge/calendrier.

La série HCMOS commerciale de composants digitaux a été retenue à cause de leur faible coût, une plage de températures d'opération étendue (-40°C à 85°C), une bonne immunité au bruit (niveaux logiques de 2 à 6 volts), et leur faible puissance d'opération ainsi que les sources d'approvisionnement diversifiées.

2.2.4 Logiciel

Programme d'analyse de la forme d'onde

Ce programme traite le signal reçu de la tête radiomètre afin d'extraire les paramètres requis des véhicules. Ce traitement permettra de déduire la longueur du véhicule ainsi que sa vitesse d'après la forme d'onde obtenue, et d'après des paramètres tels que la forme du faisceau, la configuration géométrique et les équations du radiomètre.

Sur cette base, le processeur effectue la classification pertinente du véhicule (petites voitures, voitures, camionnettes, camions, etc). On peut visualiser ceci par une matrice où les rangées correspondent aux différentes catégories et les colonnes à l'éventail des vitesses.

	V1	V2	V3	V4	V5	TOTAL
Classe A						
Classe B						
Classe C						
Classe D						
Classe E						
						GRAND TOTAL

Chaque case contient le nombre approprié de véhicules qui ont été comptés. La dernière colonne correspond au total pour chaque groupe de véhicules.

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Interface de communication

Pendant son fonctionnement local, le micro-contrôleur traite le signal, met à jour les statistiques et emmagasine les résultats. Lorsqu'il reçoit une demande de l'ordinateur central, le programme de communication exécute des actes tels que:

- vérifier si l'adresse transmise correspond ou non à sa propre localisation;
- décoder et identifier le message;
- prendre la décision appropriée pour extraire, selon le format approprié, l'information requise emmagasinée en mémoire;
- transmettre la réponse, selon le protocole de communication utilisé;
- contrôler le format et vérifier les caractères du message transmis;
- transmettre les mots de statut et de protocole afin de compléter l'échange d'information.

CRIQ

3 SPÉCIFICATIONS TECHNIQUES ET FONCTIONNELLES

3.1 Fonctions et performances

L'instrument, lorsqu'il est installé à une hauteur adéquate au-dessus d'une voie d'autoroute à voies multiples, doit compter les véhicules qui passent dans cette voie particulière.

En outre, l'instrument doit classifier le véhicule dans une des cinq catégories possibles et emmagasiner cette information en mémoire. De plus, il doit fournir une mesure de la vitesse du véhicule.

Le taux d'erreurs dans le comptage des véhicules est de moins de 1%.

En ce qui a trait aux erreurs de classification, il y a moins d'une classification erronée pour dix (10) classifications correctes.

Catégories de véhicules typiques:

-4,5 m	(-14 pieds)	- "petites voitures"
4,5-6,0 m	(15-18 pieds)	- "grosses voitures"
6,0-9,0 m	(19-28 pieds)	- "petits camions"
9,0-12,5 m	(29-40 pieds)	- "camions moyens"
12,5-20 m	(41- + pieds)	- "gros camions - camions remorques"

Catégories de vitesses typiques:

i.e.	3-15 kmh	(2-10 mph)
	15-30 kmh	(10-20 mph)
	30-60 kmh	(20-40 mph)
	60-110 kmh	(40-70 mph)
	110 + kmh	(70 +)

La vitesse des véhicules où les conditions de température n'affecte pas le fonctionnement de l'instrument.

L'instrument a la capacité d'emmagasiner les données de mesure pour une durée allant jusqu'à 24 heures, en admettant que le nombre maximal de véhicules à l'heure soit de 2500 et que les résultats soient emmagasinés en tant que nombre de véhicules dans la catégorie de vitesse X et la catégorie de taille Y.

L'instrument incorpore les résultats sous forme de matrices. Il y a deux (2) matrices: l'une d'elle con- serve les résultats de façon cumulative et ne peut être remise à zéro que par la commande de l'ordinateur central, l'autre matrice conserve les résultats intermédiaires ou partiels et peut être remise à zéro par une commande de l'ordinateur central.

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L'instrument a suffisamment de capacités de calcul en réserve pour permettre la modification des algorithmes de vitesse et de catégorie, et le développement d'algorithmes des conditions de la route.

3.2 Construction physique

L'instrument est logé dans un boîtier robuste à l'épreuve des conditions climatiques et compatible avec une installation extérieure, dans les conditions climatiques particulières au Canada. Un "radome" protège l'antenne.

Toutes les connexions sont faites en fonction d'un aménagement pour un débranchement rapide. L'instrument est supporté par un adaptateur afin de permettre un retrait rapide pour la maintenance et adaptable aux différents suppors ou structures de viaduc, pont, etc...

Les connecteurs électriques utilisés dans l'appareil sont pour:

. l'alimentation en pouvoir DC (+24V), l'interface de communication RS-232C ainsi que l'interface de communication RS-422 utilisent un connecteur militaire de type MS-3120E-16-26S;

. le signal de "température" non traité est disponible par l'intermédiaire d'un connecteur BNC de type Amphenol UG-492A/U-1050.

3.3 Pouvoir d'alimentation électrique

L'instrument opère à partir d'une alimentation en pouvoir DC de 24 $\pm$ 2V à 2A maximum.

Les bruits et l'ondulation sur l'entrée de l'alimentation DC ne devront pas excéder deux (2) volts crête à crête. L'instrument inclut une protection transitoire adéquate.

3.4 Signaux d'entrées et de sorties

. Signal de "température" non-traité (analogue)
. Lien de communication série RS-232C (digital) (taille et vitesse du véhicule)
. Lien de communication série RS-422 (digital) (données accumulées de taille, de vitesse et de nombre)
. Alimentation (+24 $\pm$ 2V à 2A max.)

3.5 Interface de communication

a) Analogue; une sortie est disponible pour le signal de "température" analogue.

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b) RS-232C (digital); l'interface de communication série RS-232C, est une interface de sortie seulement ("Transmit only", du senseur de véhicules vers l'extérieur). Après chaque détection de passage d'un véhicule, sur la voie d'observation, l'appareil transmet, par l'intermédiaire de cette interface, l'heure présente et l'information déduite, c'est-à- dire la vitesse et la taille du véhicule observé.

. Canal de communication:

- Niveau RS-232C
- Transmission (sortie seulement)
- Asynchrone
- Caractère ASCII, 7 bits, 1 start, 2 stop, parité impaire
- Taux ajustable 300 à 9600 bauds

. Format du message:

- Bell (07H)
- Heure présente, avec le format HH/MM
- SP (20H)
- Trois (3) caractères ASCII donnant la vitesse du véhicule en milles/heure
- SP (20H)
- Deux (2) caractères ASCII donnant la longueur en pieds du véhicule. Si la longueur du véhicule est plus grande que 99 pieds, alors le premier caractère correspond à une lettre qui identifie le nombre de dizaine de pieds (A = 10, B = 11..., Z = 26).
- LF (0AH)
- CR (0DH)

c) RS-422 (digital); l'interface de communication RS-422 transmet les données accumulées de taille, de vitesse et de nombre, sur commande, d'une source locale ou éloignée (pour détail, voir section 3.8: Protocole de communication).

3.6 Algorithmes de calcul

Les algorithmes pour les calculs de taille et de vitesse sont d'abord expérimentaux et sont facilement modifiables dans les prototypes.

On étudiera, en utilisant les prototypes, un algorithme de détection des conditions de la route (mouillée, sèche, glacée, etc.).

CRIQ CENTRE DE RECHERCHE

3.7 Conditions environnementales

L'unité fonctionne à l'intérieur des limites de cette spécification à une température ambiante de -40°C à +60°C et résiste à des expositions prolongées à des températures aussi basses que -40°C et aussi élevées que +100°C, sans encourir de dommage permanent. Le senseur de véhicules opère de façon satisfaisante dans des conditions d'humidité relative allant jusqu'à 100%, ceci incluant la condensation et les précipitations.

3.8 Protocole de communication avec l'ordinateur central

Canal de communication

- Niveaux RS-422
- Half-Duplex
- Asynchrone
- Caractères ASCII, 7 bits, 1 start, 1 stop, parité impaire
- Taux ajustable 110 à 9600 bauds

Contrôle de la communication

- L'ordinateur central interroge ou commande le détecteur du véhicule.
- Le senseur répond à la demande.
- L'ordinateur central contrôle les communications et voit aux retransmissions.

Le format des messages est le suivant:

Ordinateur central	Senseur de véhicules
- SOH (01H)	- SOH (01H)
- Adresse appelée (1 caractère ASC11:0-9)	- Adresse répondeur (1 caractère ASC11:0-9)
- ENQ (05H)	- STX (02H)
- Message	- Message
- ETX (03H)	- ETX (03H)
- BCC, Parité longitudinale (LPC)	- BCC (LPC)
- EOT (04H)	- EOT (04H)

Les différentes demandes de l'ordinateur (et leurs réponses) sont les suivantes. (N.B.: On ne présente que la partie message puisque le format est le même pour tous les messages.)

CRIQ CENTRE DE RECHERCHE INDUSTRIELLE DU QUÉBEC

A- Total cumulatif des véhicules, depuis la remise à zéro de la mémoire cumulative.

Demande	Réponse
- T (pour total) (54H)	- T
- C (pour cumulatif) (43H)	- C
	- 5 caractères (5 digits du MSB ou LSD)

B- Total (partiel) des véhicules, depuis la dernière remise a zéro de la matrice des résultats partiels.

- T (54H)	- T
- P (43H)	- P
	- 5 caractères ASCII

C- Sous-totaux cumulatifs par catégorie de longueur, ou regroupement de longueurs (regroupement maximum de 2 catégories à la fois)

- S (sous) (53H)	- S
- T (total) (54H)	- T
- C (cumulatif) (43H)	- C
- 2 caractères ASCII indiquant le regroupement de catérorie de longueur	- 2 caractères ASCII - / - 5 caractères ASCII pour le nombre de véhicules
- S autres sous-totaux	- S autres sous-totaux
- T si nécessaire	- T si nécessaire
- C	- C
.	- .
.	- .
.	- .

D- Sous-totaux, partiels, par longueur ou regroupement de longueur.
Le message est similaire au précédent, P remplace C.

- S (53H)	- S
- T (54H)	- T
- P (50H)	- P
.	- .
.	- .

E- Détail des comptes de véhicules par catégorie de longueur et de vitesse, résultats cumulatifs.

- D pour détail (44H)	- D détail (44H)
- C pour cumulatif (43H)	- C cumulatif (43H)
	- L longueur (4CH)
	- 1 (31H)
	- V vitesse (56H)

- 1 (31H)
- / (2FH)
- 5 caractères ASCII pour le nombre de véhicules
- L longueur
- 1 1
- V vitesse
- 2 2
- /
- 5 caractères ASCII
  .
  .
- L
- 5
- V
- 5
- /
  5 caractères ASCII pour le nombre de véhicules
- L
- 5
- V
- 5
- /
- 5 caractères ASCII pour le nombre de véhicules

F- Détail des comptes de véhicules, résultats partiels. Le message est similaire au précédent, P remplace C.

- D
- P

- D
- P
- L
- 1
- V
- 1
- /
  .
  .
  .

G- Remise à zéro de la mémoire cumulative

- R (remise à zéro) (52H)
- M (mémoire) (4DH)
- C (cumulative) (43H)

- R
- M
- C

CRIQ CENTRE DE RECHERCHE INDUSTRIELLE DU QUÉBEC

H- Remise à zéro de la mémoire de résultats partiels

- R (52H)	- R
- M (40H)	- M
- P (50H)	- P

I- Lecture de l'horloge et du calendrier interne, système 24 heures.

- Y (year) (79H)	- Y
- M (mois) (4DH)	- 2 caractères ASCII, pour l'année
	- M
- D (date) (44H)	- 2 caractères ASCII pour le mois
- H (heure) (48H)	- D
- M (minute) (4DH)	- 2 caractères ASCII pour la date
- S (seconde) (53H)	- H
	- 2 caractères, ASCII pour heure
	- M
	- 2 caractères ASCII pour minute
	- S
	- 2 caractères ASCII pour seconde

J- Remise à date de l'horloge et du calendrier interne. Le senseur répond par la date et l'heure que l'ordinateur lui a envoyées.

- Y (année) (79H)	- Y
- 2 caractères ASCII pour l'année	- 2 caractères ASCII
- M (mois) (4DH)	- M
- 2 caractères ASCII pour le mois	- 2 caractères ASCII
- D (date) (44H)	- D
- 2 caractères ASCII pour la date	- 2 caractères ASCII
.	.
.	.
.	.

K- L'état de la route est déterminé à toutes les demi-heures, et cumulé pour 24 heures. L'état de la route peut être sec (S), mouillé (M), glacé (G) ou inconnu (?).

- C (condition) (43H)	- C
- R (de la route) (52H)	- R

CRIQ

- S, M, G ou ? (état 23½ heures plus tôt)
- S, M, G ou ? (23 heures plus tôt)
.
.
.
- S, M, G ou ? (état le plus récent)

L- Lecture de la queue d'information. Après chaque passage d'un véhicule sous le détecteur, l'information correspondante est emmagasinée dans une queue. L'information contenue actuellement dans la queue est lue sur demande de l'ordinateur central.

- Q (queue) (51H)	- Q
- I (information) (49H)	- I
	- 9 caractères ASCII pour l'information concernant le 1er véhicule avec le format, HH:MM: type (1 à 5): Vitesse (1 à 5)
	- / (2FH)
	- 9 caractères ASCII pour l'information du 2e véhicule
	- /
	- .
	- .
	- / (2FH)
	- 9 caractères ASCII pour l'information du dernier véhicule contenu dans la queue

M- Remise à zéro de la queue d'information

- R (remise à zéro) (52H)	- R
- Q (queue) (51H)	- Q
- I (information) (49H)	- I

CRIQ

4 DESCRIPTION D'OPÉRATION, D'ENTRETIEN ET DE DÉPANNAGE

4.1 Schéma bloc, alimentation et mécanique

La figure 5 montre les principaux modules électroniques de l'appareil. A l'appendice A.1 se trouve un dessin montrant les différentes interconnexions entre chacun des modules électroniques.

L'appareil est composé de huit (8) modules électroniques, le tout contrôlé par un logiciel. Les huit (8) modules électroniques sont:

. l'alimentation,
. le radiomètre,
. la carte audio,
. la carte convertisseur analogue à digital (LPM-A/D),
. la carte microprocesseur (78C15),
. la carte calendrier/horloge (MCM-CLK),
. la carte de communication (73C04),
. la carte entrées/sorties (79C04).

Chacun de ces modules est décrit dans une section de ce rapport.

4.1.1 Mécanique

Le boîtier extérieur est un boîtier Hammond, modèle 1414N4PHM8. Ce boîtier de 8" X 12" X 14" est de type étanche à l'eau.

Les cartes électroniques répondent aux spécifications mécaniques STD 70C00. Une description détaillée des spécifications mécaniques de ces cartes est reproduite à l'appendice A.2

Le support de cartes est de type STD Pro-Log, modèle BR08-H. Une description ansi que les spécifications mécaniques de ce support de cartes sont reproduits à l'appendice A.3.

Les connecteurs électriques utilisés par l'appareil sont pour:

. L'alimentation en pouvoir DC (+24), les interfaces de communication RS-232-C ainsi que RS-422 utilisent un connecteur militaire de type MS-3120E-16-26S.

. Le signal de "température" non traité est disponible par l'intermédiaire d'un connecteur BNC de type Amphenol UG-492A/U-1050.

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4.1.2 Alimentation

L'instrument opère à partir d'une alimentation en pouvoir DC de 24 ±2V à 2A maximum.

A l'appendice A.4 se trouve le schéma électrique de l'alimentation.

A partir de l'alimentation 24 volts de l'entrée, des convertisseurs DC/DC et d'un régulateur, nous fabriquons les alimentations nécessaires aux circuits électroniques.

Le convertisseur DC/DC, modèle UM13-100-24 de la compagnie Power Source Semiconductor Circuit Inc., transforme le +24 volts en +15 volts. Cette tension est nécessaire au module radiomètre. Du voltage 15 volts, nous dérivons à l'aide d'un régulateur (7805), le voltage 5 volts dont le radiomètre a aussi besoin.

Un second convertisseur DC/DC, modèle UM11-300-24 de la compagnie Power Source Semiconductor Circuit Inc., fournit le +5 volts aux cartes électroniques.

Le ±12 volts requis par les cartes électroniques est fourni à l'aide du convertisseur DC/DC, modèle N24D12/330X, de la compagnie Stevens-Arnold Power Products.

Les spécifications des convertisseurs DC/DC utilisés se touvent à l'appendice A.5.

4.2 Radiomètre

Ce module a été sous-contracté à "Antenne Technologie Antech Ltée". Cette compagnie a été ultérieurement acquise par la compagnie COM DEV Ltd.

Vous trouverez à l'annexe B le rapport fourni par le sous-contractant concernant l'opération, l'entretien et le dépannage de ce module.

4.3 Carte audio

Ce module a été réalisé par le CRIQ. Les schémas électriques de cette carte sont présentés à l'appendice C.

Le signal de sortie du radiomètre est amplifié dans un amplificateur "audio" de 50 db de gain et faible bruit. La bande de fréquences est de 100 Hz à 10 kHz.

Après amplification, le signal du radiomètre est détecté de façon synchrone (U1) avec le commutateur d'antenne du

radiomètre, pour obtenir une variation D.C. proportionnelle à la différence de température entre la charge de référence et celle vue par l'antenne. Un amplificateur opérationnel (U2) permet un ajustement de gain et d'offset.

Un filtre passe-bas ("low pass") est réalisé à l'aide de l'amplificateur U3. Le filtre a un gain total de 1 et une bande passante de 15,6 Hz à -3 dB. Le filtre est linéaire de phase de 0 à 16 Hz. Ce signal de "température" non traité est disponible à l'extérieur du boîtier par l'intermédiaire d'un connecteur BNC de type Amphenol UG-492 A/U-1050. Ce signal est acheminé par l'intermédiaire du connecteur J2 à la carte convertisseur analogue à digital.

Un senseur de température (Q6) fournit une tension proportionnelle à la température des circuits, à l'intérieur du boîtier, en vue d'une correction de calculs en fonction de la température d'utilisation.

4.4 Carte convertisseur analogue à digital

Cette carte réalise la conversion de signaux analogue à digital. Elle réalise cette conversion pour le signal de "température" de la route et pour le signal venant du senseur de température interne, ces deux signaux venant de la carte audio.

Ce module est réalisé par la carte, modèle LPM-A/D de la compagnie Wintech Systems Inc. A l'appendice D se trouve le manuel d'opération fourni par le manufacturier de cette carte.

Les adresses (en hexadécimal) des entrées/sorties de cette carte sont de 3C à 3E (aucun cavalier sur J6).

Les entrées analogues sont de type différentiel (cavalier sur J2: entre 1 et 4 et entre 2 et 3, cavalier sur J3: entre 1 et 3 et entre 3 et 4).

La plage des signaux d'entrées doit être comprise entre +5 volts (cavalier sur J5: entre 5 et 6 et entre 7 et 8).

Le signal venant du senseur de température interne est appliqué sur le canal Ø (J1-1: chan Ø(+), J1-14: chan Ø(-), alors que le signal de "température" de la route est appliqué sur le canal 7 (J1-13: chan 7(+), J1-26: chan7(-).

Cette carte ne génère pas d'interruption du micro-ordinateur (aucun cavalier sur J7).

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Les tensions ±12 volts sont fournies par l'intermédiaire du connecteur (alimentations extérieures: cavalier sur J9: entre 1 et 2 et entre 3 et 4). Le signal de masse analogue vient de l'extérieur (cavalier sur J8: entre 1 et 2).

La sortie digitale de cette carte est de type "offset binary" (cavalier sur J4: entre 3 et 4).

4.5 Carte CPU

Le module micro-ordinateur est réalisé à l'aide de la carte 78C15 de la compagnie Pro-Log. A l'appendice E se trouve le manuel de l'usager fourni par le manufacturier.

Tous les cavaliers doivent être à la position telle que livré par le manufacturier (voir figure 2-3 page 2-5 du manuel de l'usager, appendice E).

La mémoire EPROM (mémoire Ø, U8) est de type 2764A et a une capacité de 8K * 8. La mémoire vive (RAM) est une puce de Harris (HM-6516) et a une capacité de 2K * 8 (mémoire 1, U7). Pour que cette mémoire RAM puisse fonctionner, il faut installer celle-ci sur les broches 3 à 26 inclusivement sur le support de 28 broches et installer un cavalier entre les broches 27 et 23, de ce support de puce (c'est-à-dire que la broche 21 de la puce doit recevoir le signal $\overline{CWR}$). La broche 5 de la puce U21 doit aussi recevoir le signal ALE et non le signal PD2.

Le microprocesseur 8025 peut être interrompu par deux signaux. L'interruption $\overline{RST\ 7.5}$ est causée par une horloge à toute les 10 ms, cette horloge est située sur la carte d'entrées/sorties. L'interruption $\overline{RST\ 6.5}$ est causée par la réception d'un caractère venant de l'interface RS-422.

4.6 Carte calendrier/horloge

Cette carte réalise les fonctions d'horloge et de calendrier. Cette carte est fabriquée par la compagnie Wintech Systems Inc. Le manuel d'opération de cette carte se trouve à l'appendice F.

Cette carte ne contient pas de batterie, à cause des basses températures d'opération de l'appareil. Il faut donc initialiser l'appareil avec l'heure et la date à chaque fois que nous alimentons l'appareil, sinon l'appareil prend par défaut l'heure 00:00:00 et la date 1er jour du 1er mois de l'année 00.

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Les adresses (en hexadécimal) des entrées/sorties de cette carte sont comprises entre 40 et 5F (cavaliers sur J4: entre 1 et 2 et entre 3 et 4).

Cette carte ne contient pas de batterie donc aucun cavalier se trouve sur J2.

Cette carte ne génère pas d'interruption (aucun cavalier sur J3).

4.7 Carte de communication

Ce module est réalisé à l'aide de la carte 73C04 de la compagnie Pro-Log. Le manuel de l'usager fourni par le manufacturier est reproduit à l'appendice G.

Les adresses (en hexadécimal) des entrées/sorties de cette carte sont situées entre EØ et E7 inclusivement (cavalier sur SX: entre 7 et 8 et cavalier sur SY: entre 9 et 10).

Le canal B est utilisé pour la communication, série RS-232-C, ce canal est utilisé en mode DTE ("Data Terminal Equipment"). Le support de programmation pour le canal B est donc installé entre XB1 et XB2. Les signaux RS-232-C sont acheminés par l'intermédiaire du connecteur J1 au connecteur militaire pour liaison avec l'extérieur.

La plage de sélection du taux de transmission et de réception ("Baud rate range") est telle qu'installée par le manufacturier (cavalier W1: entre 3 et 4, cavalier sur W2: entre 3 et 4 et cavalier sur W3: entre 1 et 2) et permet un taux de 110 à 9600 bauds.

Le canal A est utilisé pour la communication, série RS-422 et comme DTE ("Data Terminal Equipment"). Le support de programmation pour le canal A est donc installé entre XA1 et XA2. Le canal A doit être de type RS-422, il a donc fallu enlever les puces ("chips") U17 et U18 (ceux-ci font la translation des signaux TTL à RS-232C) et placer les cavaliers suivants:

U17-9 à U18-6 ARTS = ACTS
U17-4 à U18-8 ADTR = ADSR
U17-12 à U17-11 ATD = AITD
U18-1 à U18-3 ARD = AIRD

Les translateurs de niveaux TTL à RS-422 sont situés sur la carte d'entrées/sorties. Le canal A envoie donc les données par le signal de "Data Transmit" (TD, J3-3) et reçoit les données par la ligne "Receive Data" (RD, J3-5) sous forme TTL, par l'intermédiaire du connecteur J3.

Ces signaux TTL sont transformés en signaux 422 par l'intermédiaire de translateur de niveaux qui sont situés sur la carte d'entrées/sorties (voir section 4.8).

Nous voulons que les signaux pouvant interrompre le microprocesseur soit de deux sources seulement; donc les lignes U16-10 à J2-4, U16-8 à J2-6, U16-12 à J2-2 et U16-6 à J2-8 sont coupées. L'interruption RST 6.5 est causée par la réception d'un caractère venant de l'interface RS-422, donc le signal RRDYA (U16-10) est branché au connecteur J2-6. L'autre source d'interruption est causée par une horloge à toutes les 10 ms, ce signal est disponible sur le connecteur J3 broche 8 et est relié à la broche 4 du connecteur J2 de façon à actionner l'interruption RST 7.5.

4.8 Carte d'entrées/sorties

Ce module est réalisé à partir d'une carte d'utilité 79C04 de la compagnie Pro-Log. Le manuel de l'usager de cette carte est reproduit à l'appendice H.1.

Les adresses (en hexadécimal) des entrées/sorties de cette carte sont situées entre 00 et 07 (cavalier sur W1 entre 1 et 2, cavalier sur W2 entre 1 et 2 et cavaliers sur W3 entre 1 et 2 et entre 5 et 6).

A l'appendice H.2 se trouve les schémas électriques des circuits qui ont été rajoutés sur la carte 79C04.

Un oscillateur à 2 kHz (U13) fournit une horloge qui est divisé par deux par le circuit intégré U14-5, de façon à obtenir une onde carrée à la fréquence de 1 kHz. Cette horloge de 1 kHz est inversée par le transistor 2N2907 et est disponible sur le connecteur à la broche no 6, cette horloge sert au détecteur synchrone sur la carte audio (voir section 4.3). Le micro peut aussi lire l'état de cette horloge par l'intermédiaire du bit 7 du port d'entrée no Ø1 ("chip" U11).

L'horloge de 1 kHz (U14-5) est inversé par la deuxième section du C.I. U14. La sortie U14-9 contrôle l'interrupteur RF du radiomètre par l'intermédiaire de la broche 50 du connecteur. Cet interrupteur RF peut cependant être forcé dans l'état 1 (sélection de l'antenne) ou dans l'état Ø (sélection de la charge) par l'interrupteur SW1 ou par l'intermédiaire du microprocesseur. Le bit 6 du port de sortie ØØ (U12-5) lorsque placé dans l'état Ø force la sélection de l'antenne alors que le bit 7 du même port de sortie force la sélection de la charge (U12-2).

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Les circuits intégrés qui font la translation de TTL à RS-422 et de RS-422 à TTL sont respectivement les circuits U8 et U9. Les signaux TTL sont acheminés par le connecteur J3 vers la carte de communication alors que les signaux 422 sont acheminés par l'intermédiaire du connecteur J2 au connecteur militaire pour connexion avec l'extérieur. Le signal de permission ("enable") du transmetteur 422 (U8-12) est contrôlé par le microprocesseur par l'intermédiaire du bit Ø du port de sortie ØØ (U12-19).

Les bits Ø à 3 du port d'entrée ØØ (U10) contiennent l'information concernant la hauteur à laquelle est installé le détecteur. La différence entre cette hauteur à laquelle le détecteur est installé et 16 pieds est programmée de façon binaire à l'aide de cavaliers sur W4.

Les bits 4 à 6 du port d'entrée 00 servent à identifier l'adresse du détecteur. L'adresse du détecteur doit être située entre Ø et 7 et doit être unique. Cette adresse est programmée de façon binaire à l'aide de cavaliers sur les trois premières positions de W5.

L'angle d'inclinaison du détecteur doit être de 0° ou de 30°. Cette information est fournie au microprocesseur par l'intermédiaire du bit 7 du port d'entrée 00 (U10-17) et de la dernière position sur W5. Un cavalier sur la dernière position de W5 indique un angle d'inclinaison de 0° pour le détecteur alors qu'une absence de cavalier indique un angle d'inclinaison de 30°.

La sélection de la vitesse de communication du canal B se fait par l'intermédiaire de cavalier sur les trois premières positions de W6, alors que la vitesse du canal A est réalisée par l'intermédiaire des trois dernières positions de W6. Le port d'entrée 01 (U11) transmet ces informations au microprocesseur.

Programmation sur W6 (MSB, 2e bit, LSB)			Vitesse sélectionnée (Bauds)
0	0	0	110
0	0	1	150
0	1	0	300
0	1	1	1200
1	0	0	1800
1	0	1	2400
1	1	0	4800
1	1	1	9600

N.B.: Sur cette carte, la convention ci-dessus s'applique:

0: cavalier reliant les deux broches (ex: cavalier sur W4 entre 1 et 2),
1: pas de cavalier.

L'horloge de 1 kHz, c'est-à-dire l'horloge avec une période de 1ms est divisée par 10 par l'intermédiaire de U16. Cette horloge interrompt le microprocesseur à toutes les 10 ms de façon à ce que le microprocesseur analyse à ce rythme les informations venant du senseur à micro-ondes.

4.9 Logiciel

Le logiciel ou programme pour réaliser les spécifications décrites à la section 3.0 se trouve à l'appendice I.

Ce programme est écrit en langage PL/M-80. Le programme source est disponible sur disquette 5¼", format INTEL ISIS-IPDS.

Ce programme est documenté par lui-même puisqu'il est réalisé par module et qu'il contient plusieurs commentaires.

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5 RÉSULTATS, CONCLUSIONS ET RECOMMANDATIONS

Les essais ont démontré que l'on peut utiliser un système à radiomètre pour compter, classifier par catégories et connaître la vitesse et la longueur des véhicules se déplaçant sur une autoroute. L'état de la surface (sec, mouillé ou glacé) de la route peut aussi être connu par l'intermédiaire de l'appareil.

Les résultats des essais ont démontré que cette technologie était très fiable pour détecter la présence ou pour compter les véhicules; le taux d'erreurs dans le comptage est de moins de 1%.

Les essais ont aussi permis de vérifier que l'information concernant la taille (longueur) et la vitesse des véhicules pouvait être déduite avec une bonne précision.

La majorité des erreurs sont dues au fait que certains véhicules sont couverts, en partie seulement, de métal et par conséquent ne réfléchissent que sur cette partie de leur longueur la températurure du ciel (exemple: camion avec plate-forme de bois, camion semi-remorque avec chargement recouvert d'une toile).

La classification des véhicules est aussi très difficile à réaliser pour certaines catégories de véhicules. La distinction entre la classe des petites automobiles et des grosses automobiles est réalisée sur quelques pieds et même un observateur a beaucoup de difficulté à classifier certains véhicules. La même remarque s'applique lors de la classification de camionnettes, de camions de livraison et de petits camions de services.

Les essais effectués ont été réalisés sur une période de temps limité. Il faudrait donc réaliser des essais sur une période prolongée et réaliser, en parallèle à ces essais, une étude statistique des résultats de l'appareil en fonction du type de véhicule et de l'état des conditions climatiques environnantes. Il y aurait lieu aussi de réaliser des essais sur plusieurs sites différents mais sur une période de temps beaucoup plus courte.

Les algorithmes actuels sont de types expérimentaux et devraient être revus en fonction des résultats obtenus lors de ces essais.

Des travaux supplémentaires de R & D devraient être entrepris pour améliorer l'appareil. A ce titre, il faudrait investiguer la possibilité de réduire le faisceau de l'antenne. Cette approche nous donnerait une

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meilleure précision pour les petits véhicules tout en ne modifiant pas la précision pour les autres catégories de véhicules. Les algorithmes devraient cependant être modifiés en fonction de cette nouvelle antenne.

Les présents prototypes sont des modèles d'exploration. Il faudrait donc des travaux supplémentaires de développement pour aboutir à un modèle de production. Des discussions avec certaines entreprises hautement expérimentées dans le domaine des composants micro-ondes ont démontré qu'il est possible de produire le composant micro-onde en grande quantité et à faible coût. Il est donc réaliste de penser que le senseur de véhicules, dans une version de production, pourrait se vendre aux environs de mille dollars par unité, ce qui en ferait un senseur très compétitif au point de vue prix par rapport aux autres senseurs tout en offrant des caractéristiques et possibilités accrues.

On peut donc espérer que l'expérience et les essais futurs réalisés avec ces prototypes mèneront à l'élaboration d'un produit commercial de haute technologie pour l'industrie canadienne, et offriront des caractéristiques et des possibilités énormes pour le domaine du contrôle de la circulation et du transport.

APPENDICE A

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A.1 SCHÉMA D'INTERCONNEXIONS

A.2 SPÉCIFICATION 70C00

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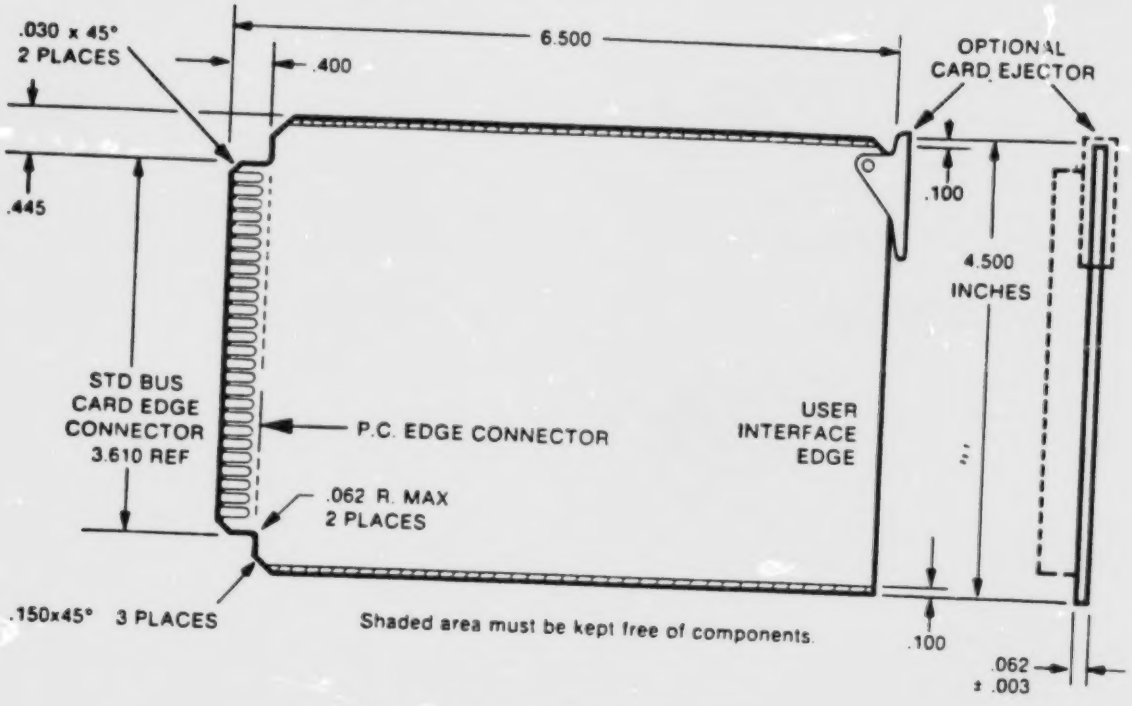


Figure 1-2. STD BUS Card Outline — Inches

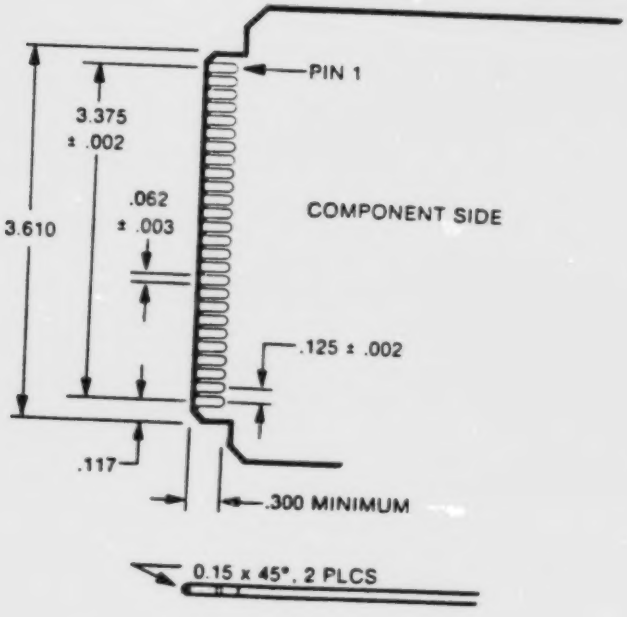


Figure 1-3. STD BUS Card Edge Finger Design — Inches

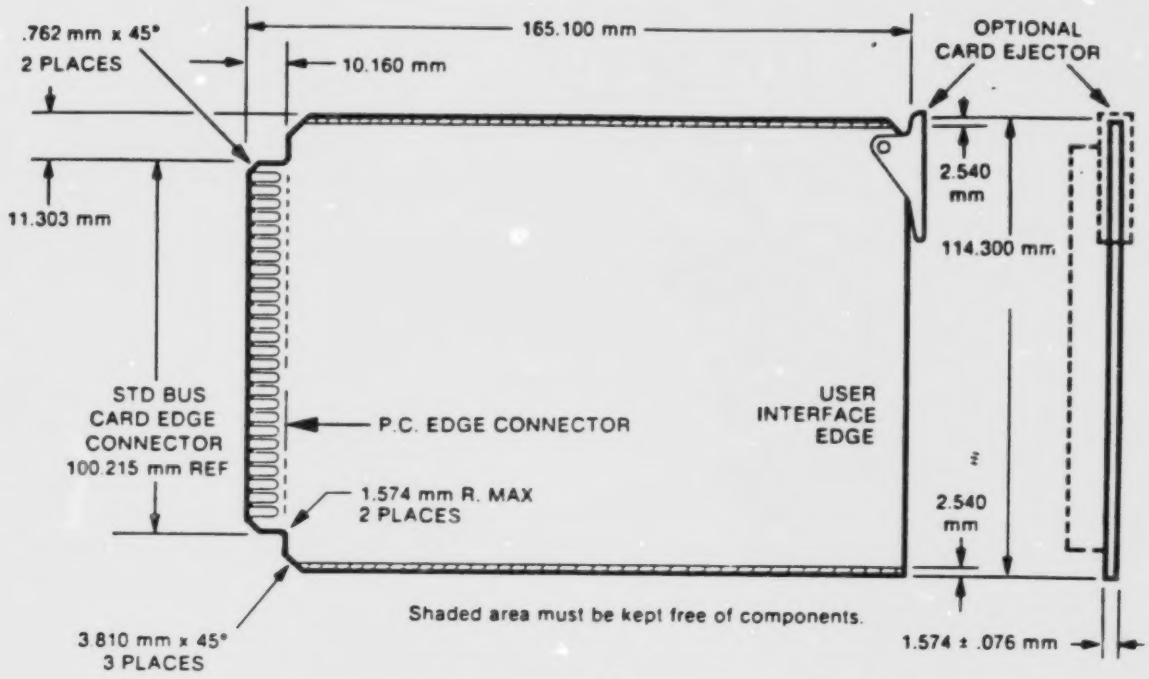


Figure 1-4. STD BUS Card Outline — Metric

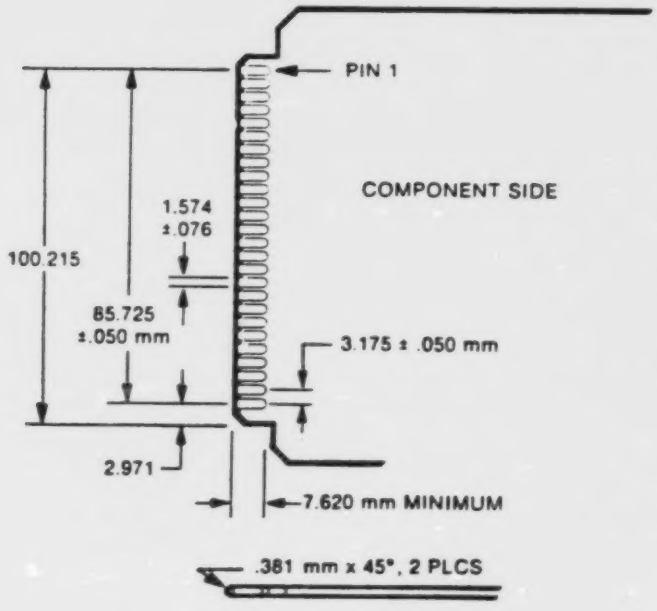


Figure 1-5. STD BUS Card Edge Finger Design — Metric

MATERIALS

The card base material is natural epoxy-impregnated novenglass with a flammablity rating of 94V-1 on 94V-0. The conductors on the finished boards are at least 2.4 mil thick. The contact fingers have at least 30 μ-inches of gold over 200 μ-inches of nickel (MIL-G-45204).

ENVIRONMENTAL SPECIFICATIONS

TTL

- Operating temperature: 0° to 65°C typically
- Storage temperature: -40° to +75°C typically
- Operating humidity: 5 to 95% noncondensing relative humidity
- Nonoperating humidity: 5 to 95% noncondensing relative humidity

CMOS

- Operating temperature: -40° to +85°C typically
- Storage temperature: -40° to +100°C typically
- Operating humidity: 5 to 95% noncondensing relative humidity
- Nonoperating humidity: 5 to 95% noncondensing relative humidity

For additional thermal considerations refer to Pro-Log Application Note PLAN 133, "Thermal Application Note for Microprocessor Systems."

ELECTRICAL SPECIFICATIONS

The Series 7000 cards meet the STD BUS specifications including absolute maximum ratings, power supply voltages, logic signal characteristics, and standard bus unit loads. Details of the electrical standards for the CMOS STD BUS are being developed.

On TTL cards, low-power Schottky (LSTTL) support logic and buffering are used to give the cards low input loading and low power consumption, without sacrificing speed or output drive capability. Most cards use LSTTL buffers with 200 mV of hysteresis for noise immunity. For further considerations on power and grounding, refer to Pro-Log PLAN 134, "Power and Grounding Considerations for STD BUS Systems."

On CMOS cards, CMOS logic is used wherever possible with high-speed CMOS (74HCXXX) used for all support logic and buffering.

To determine the number of STD BUS cards possible in a system, total the number of input loads (STD unit loads) on each bus line. Each output driver on the same line must be capable of driving at least that number of loads. The data for each card is available from the specific card's data sheet and user's manual.

SERIES 7000 STD BUS TIMING

For card timing information, refer to the individual data sheets and user's manuals.

CARD ADDRESSING OPTIONS

User addressing options are made by a jumper selection on all processor, memory, and I/O cards, which allow the user to permanently change the address of the card and on-card elements such as memory chips and ports. Refer to the user's manuals for specific address mapping options and procedures.

A.3 SUPPORT DE CARTES

STD BUS
BR-, ER-, & WR-SERIES
CARD RACKS

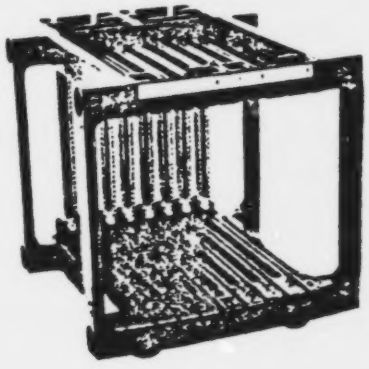
The Pro-Log card racks are assembled from modular elements, allowing the designer a wide choice of rack designs. The four-slot card-rack modules are made from injection molded, glass filled thermoplastic polycarbonate. They are assembled with mounting hardware in 36 models. This allows a wide range of card rack implementations.

These card racks accept all 4.5 by 6.5 in. (114.3 x 165.1 mm) STD BUS circuit cards and feature excellent convection cooling.

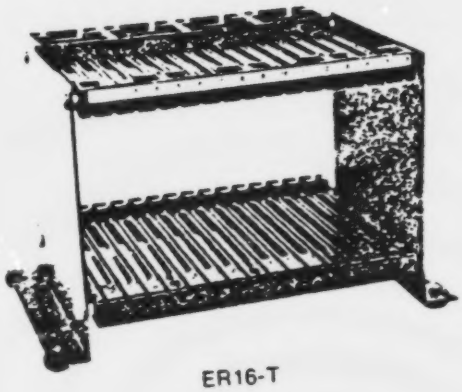
Card spacing is on 0.5 in. (12.7 mm) centers, except for the BR24 models, which have 16 card slots on nominal 0.5 in. (12.7 mm) centers and 8 card slots on nominal 1.0 in. (25.4 mm) centers.

FEATURES

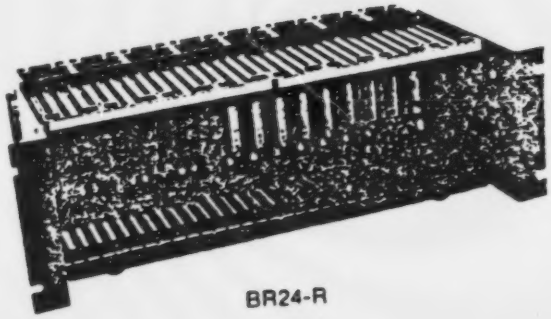
- Accepts all STD BUS cards
- Available in 4, 8, 16, 24, and 32 card slot configurations
- Card spacing on 0.5 in. (12.7 mm) centers (except BR24)
- Rugged, glass-filled thermoplastic construction
- Variety of mounting options: top, bottom, front, rear and sides
- Variety of card-edge connector options: bused motherboards, wirewrap, or no connectors
- Wide temperature range: -40 to +85°C
- Two-year warranty



WR8-H



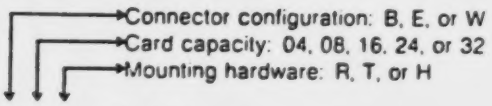
ER16-T



BR24-R

Model Number

The Pro-Log card racks are designated by a model number according to the following scheme:



xRnn-m (Model Number)

The following three tables explain each of the options available. A table on the last page of this data sheet shows all combinations of options and model numbers.

Connector Configurations

The card racks are available in three connector configurations:

PREFIX	CONFIGURATION
BR	Edge-connectors, bused motherboard, and power cable installed
WR	Unwired 56-pin wirewrap card-edge connectors installed
ER	No card-edge connectors installed

Card Capacity

The card capacity is indicated by the numerals in the middle of the model designation.

NUMBER	CAPACITY	COMMENTS
04	4	Available in all models
08	8	Available in all models
16	16	Available in all models
24	24	BR models only
32	32	WR and ER models only

Mounting Hardware

Three mounting options are available, designated by the suffix:

SUFFIX	MOUNTING HARDWARE
-R	RETMA type, front rack mount (1)
-T	Table mount brackets at bottom of rack
-H	Pro-Log handle mounts

(1) These units have an overall height of 5.75 in. (146.1 mm) excluding feet, and are designed to fit in a RETMA, standard 7 in. (177.8 mm) high panel space.

CARD RACK MOUNTING

The Pro-Log card racks can be used free-standing on their rubber feet, or they can be attached to a chassis or cabinet in a variety of ways.

Options for All Models

1. Use the racks free-standing on the factory-installed rubber feet

or

2. Secure the racks through the holes provided on the top and bottom of the four-slot card rack modules. Four holes are provided on both the top and bottom of each module. Use #4-40 or similar self-tapping screws to secure the racks.

> **CAUTION**
>
> If the racks are mounted in this manner, provide for adequate airflow for convection cooling of the cards. Use spacers between the card racks and the panel to which they are secured, or provide openings in the panel if the racks are flush-mounted to it.

or

3. Attach the card racks through the slots on the rear faces of the four-slot card rack modules. Two slots are provided on both the top and bottom of each module.

Options for -R Models (RETMA type rack mount)

4. Mount the -R model card racks, using options 1 through 3, or mount the racks by the front mounting angle brackets. The brackets have mounting slots spaced on 4.0 in. (101.6 mm) centers on each side of the racks. These slots correspond to the standard RETMA dimensions for mounting 7 in. (177.8 mm) panels in 19 in. (482.6 mm) racks. The BR24-R, ER32-R, and WR32-R mount directly in a standard 19 in. (482.6 mm) RETMA rack.

Options for -T Models (tabletop type rack mount)

5. Mount the -T model card racks, using options 1 through 3, or mount by the bottom mounting angle brackets. Each bracket has four mounting holes, of which two are used to secure the rubber feet to the bracket.

Options for -H Models (Pro-Log handle type mount)

6. Mount the -H model card racks, using options 1 through 3, or mount them by either or both sides, using #10-32 screws to attach to the rack at the captive, threaded hexagonal inserts in the handles. The racks are shipped with all inserts on one side. But the user can reverse half of all the screws and inserts to provide two mounting points on each side, or four points on one side.

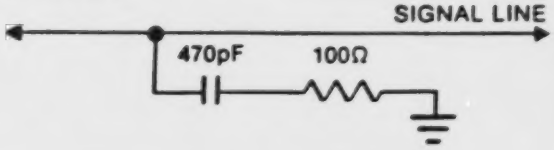
> **NOTE**
>
> The BR24, WR32, and ER32 cannot be mounted this way, since screws are used at both ends.

ENVIRONMENTAL SPECIFICATIONS

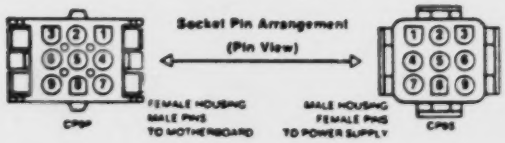
- **Free-air operating temperature: -40° to +85°C**
- **Storage temperature: -40° to +100°C**
- **Operating humidity: 5 to 95% noncondensing relative humidity**

LOGIC BUS TERMINATION
(BR24 series with 7106 motherboard only)

The Pro-Log BR24 series card racks use passive AC termination on all signal lines (pins 7 through 50) to reduce electrical ringing. Undesired high frequency ringing is effectively terminated to the characteristic impedance of the motherboard. The steady-state DC drive of each output driver is not reduced by this circuit. The following circuit represents each of the bused signal terminations.



POWER CABLE SPECIFICATIONS



SYMBOL	BUS PINS	POWER CABLE		RECOMMENDED CURRENT	
				BR04 BR08 BR16	BR24
		PINS	COLOR	MAX	MAX
VCC	1 & 2	1 & 2	Red	120	170
VBB #1	5	3	White	10	10
VBB #2	6	3	White	10	10
GND	3 & 4	4 5 6	Black	120	170
AUX +V	55	7	Orange	60	70
AUX -V	56	9	Violet	60	70
AUX GND	53 & 54	8	Wht Blk	60	70

* VBB (-5V) can be jumpered to bus pins 5 and/or 6 by user-installed jumpers on the motherboard. The BR24 comes with -5V already jumpered to bus pins 5 and 6.

MISCELLANEOUS SPECIFICATIONS

- **UL Rating: 94V-0**
- **Recommended cleaning solvent: Water or isopropyl alcohol**

ACCESSORIES

Edge Connector
Pro-Log model CW56 wirewrap edge connectors are available for use with the ER series card racks. For details, see the CW56 data sheet. User supplied connectors, such as Winchester #HW28D0-111 or equivalent, may also be used.

Motherboards
Pro-Log models 7101, 7102, 7105, and 7106 bused motherboards with soldered CW56-1 edge connectors are available for use with the ER Series card racks. For details, see the 7101, 7102, 7105 or 7106 data sheets.

Power Supply Cables
The Pro-Log model CP9P nine-pin locking power connector with a 12 in. (304.8 mm) cable is available for connecting to the WR and ER series card racks. (The cable and connector are included with BR series card racks.) A mating CP9S connector and 12 in. (304.8 mm) cable are available for use with customer-provided power supplies. For details, see the CP9P/CP9S data sheet.

REFERENCES

Card Temperature Considerations
For information on card temperature considerations, request Pro-Log Application Note (PLAN) #133, document #106257.

Power and Grounding Considerations
For information on system power and ground considerations, request Pro-Log Application Note (PLAN) #134, document #106339.

MODEL NUMBER	CARD SLOTS			MOUNTING			REPLACES	COMMENTS
	TOTAL	BUSED MOTHER-BOARD	WIREWRAP CONNECTOR	RETMA	TABLE	HANDLE		
BR04-R	4	4	0	X	—	—		7105 Motherboard[1]
BR04-T	4	4	0	—	X	—		7105 Motherboard[1]
BR04-H	4	4	0	—	—	X	CR4A-2	7105 Motherboard[1]
BR08-R	8	8	0	X	—	—		7101 Motherboard[1]
BR08-T	8	8	0	—	X	—	CR8	7101 Motherboard[1]
BR08-H	8	8	0	—	—	X	CR8A-2	7101 Motherboard[1]
BR16-R[4]	16	16	0	X	—	—		7102 Motherboard[1]
BR16-T[4]	16	16	0	—	X	—	CR16	7102 Motherboard[1]
BR16-H[4]	16	16	0	—	—	X	CR16A-2	7102 Motherboard[1]
BR24-R	24	24	0	X	—	—	CR24A	7106 Motherboard[2,3]
BR24-T	24	24	0	—	X	—		7106 Motherboard[2]
BR24-H	24	24	0	—	—	X		7106 Motherboard[2]
ER04-R	4	0	0	X	—	—		
ER04-T	4	0	0	—	X	—		
ER04-H	4	0	0	—	—	X		
ER08-R	8	0	0	X	—	—		
ER08-T	8	0	0	—	X	—		
ER08-H	8	0	0	—	—	X		
ER16-R	16	0	0	X	—	—		
ER16-T	16	0	0	—	X	—		
ER16-H	16	0	0	—	—	X		
ER32-R	32	0	0	X	—	—		
ER32-T	32	0	0	—	X	—		
ER32-H	32	0	0	—	—	X		
WR04-R	4	0	4	X	—	—		
WR04-T	4	0	4	—	X	—		
WR04-H	4	0	4	—	—	X		
WR08-R	8	0	8	X	—	—		
WR08-T	8	0	8	—	X	—		
WR08-H	8	0	8	—	—	X		
WR16-R	16	0	16	X	—	—		
WR16-T	16	0	16	—	X	—		
WR16-H	16	0	16	—	—	X		
WR32-R	32	0	32	X	—	—		
WR32-T	32	0	32	—	X	—		
WR32-H	32	0	32	—	—	X		

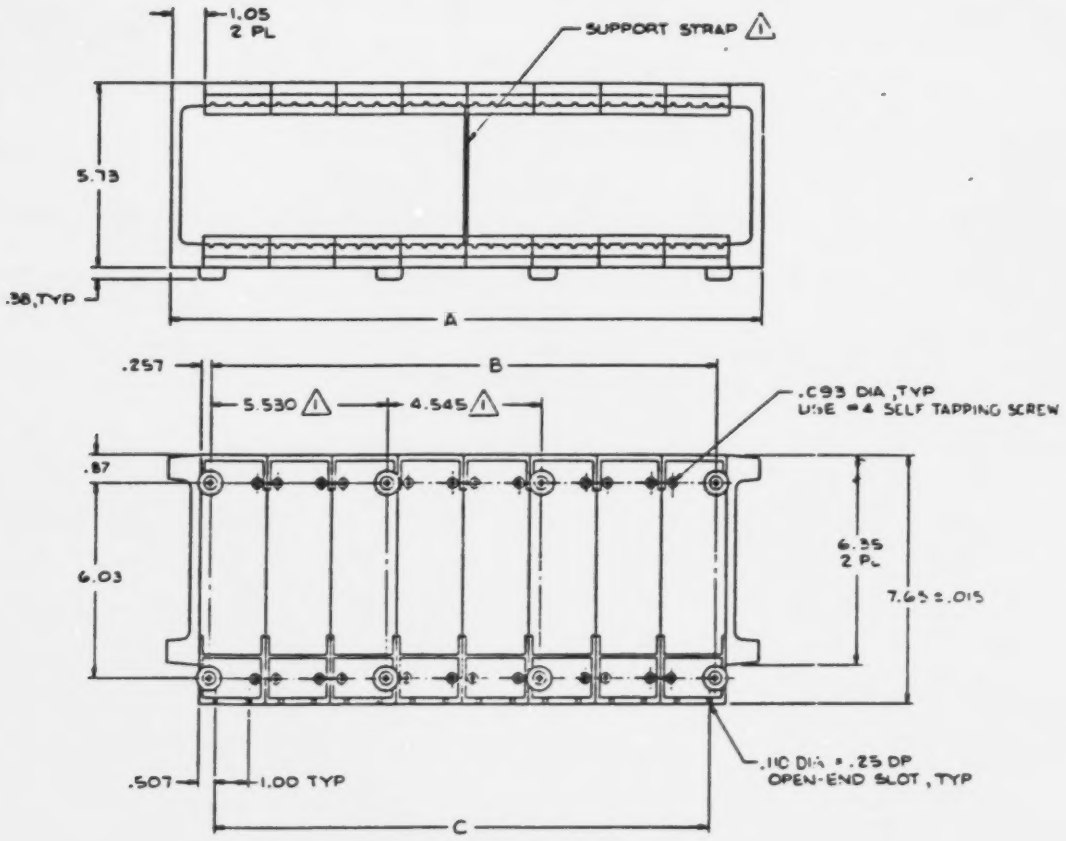
NOTES Connector keys are not included Refer to CW56 data sheet

[1] Motherboard projects about 0.25 in. (6.4 mm) past the plastic card guides, each end

[2] All BR24 model card racks have 32 card slots, of which only 24 are useable. Sixteen card slots are on nominal 0.5 in. (12.7 mm) centers and 8 card slots are on nominal 1.0 in. (25.4 mm) centers. The remaining 8 card slots are for spacing between the 1.0 in. (25.4 mm) center card slots and thus have no connectors. All BR24 model card racks include passive termination on the motherboard

[3] BR24-R, ER32-R and WR32-R card racks mount in RETMA standard 19 in. (482.6 mm) racks

[4] It is recommended that 7909A terminator card be used with these card racks



BOTTOM VIEW

FULL RACK SHOWN

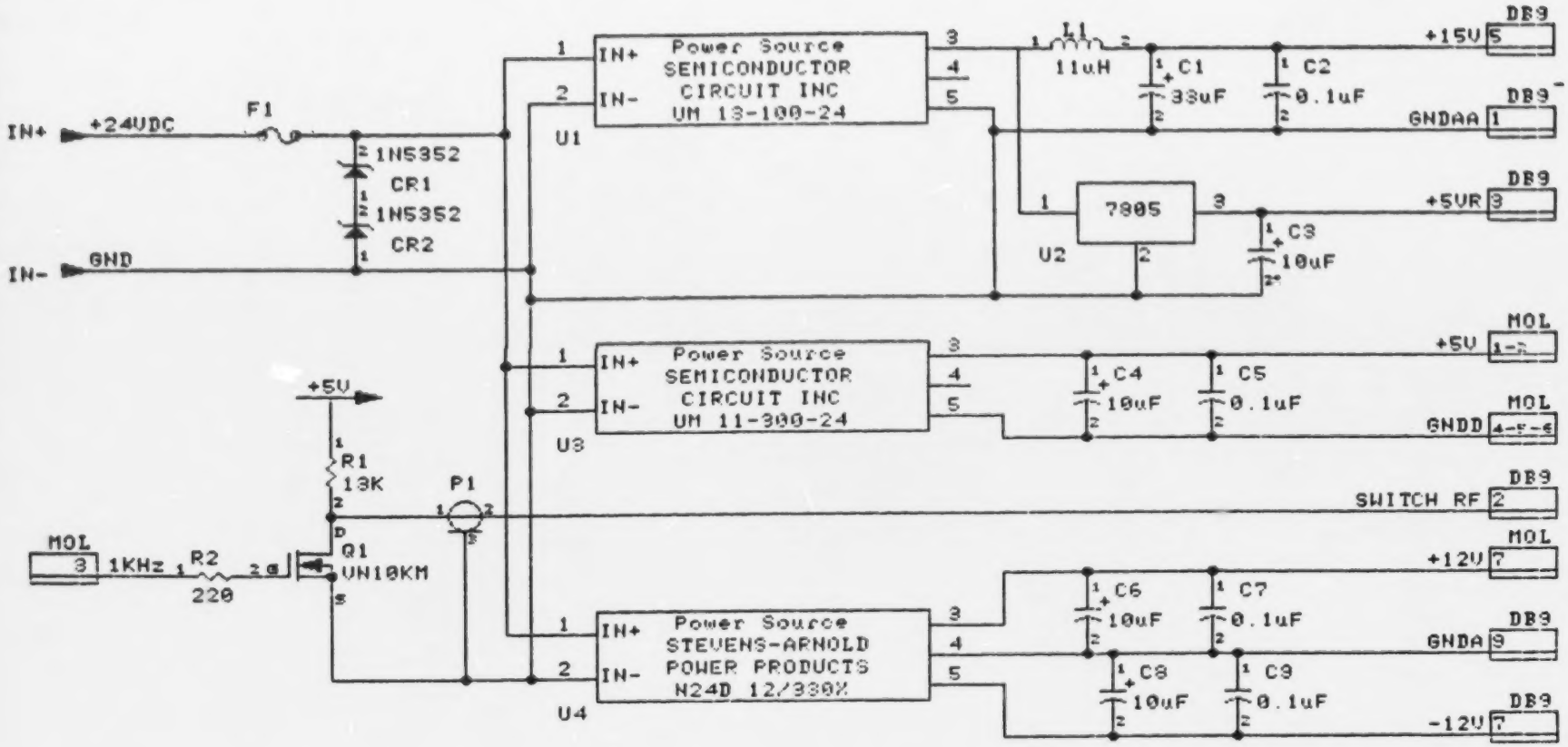
BR-H, WR-H, ER-H CARD RACK REFERENCE TABLE				
RACK SIZE	DIM A	DIM B	DIM C	TOL ±
B/E/WR04-H	4 12	1 50	1 00	065
B/E/WR08-H	6 13	3 52	3 02	070
B/E/WR16-H	10 16	7 55	7 05	080
BR24-H, E/WR32-H	18 22	15 61	15 11	100

NOTES Unless otherwise specified
1 Applies to full racks only

(in. x 2.4 = cm)

A.4 ALIMENTATION

CRIQ



DEVESU
08/04/86

SECTION 1
STD 7000 & 70C00 Specifications

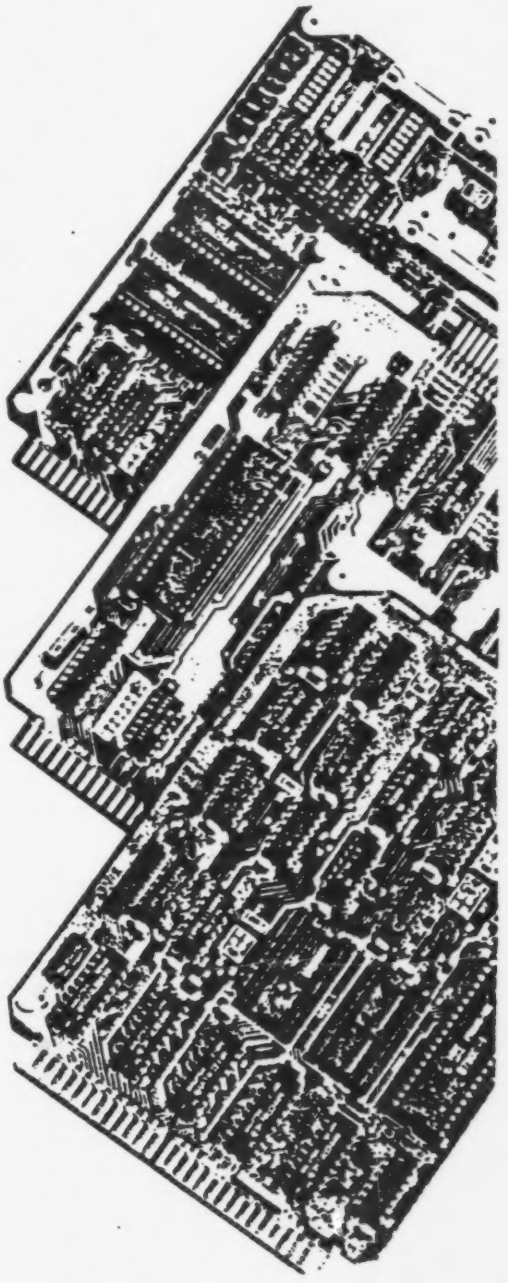
INTRODUCTION

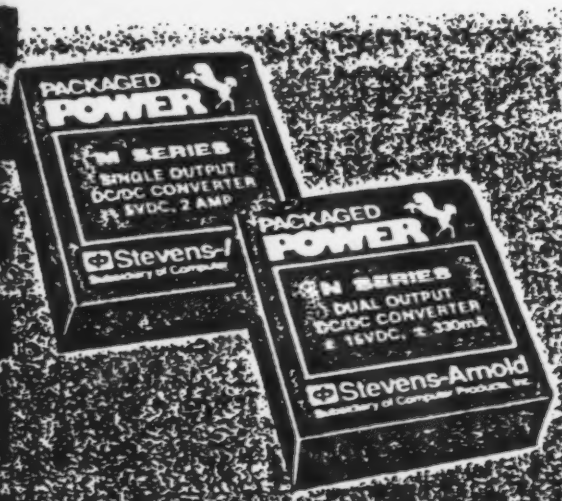
Series 7000 comprises a wide range of modular microprocessor system elements (including processor, memory cards, I/O cards, motherboards, card racks, utility cards, and power supplies), that provide high functional density with the design options needed for efficient system partitioning. The cards are divided into the following categories

- 7100 System support cards [non-4.5 x 6.5 in. (114.30 x 165.10 mm)] including motherboards
- 7300 Peripheral interface
- 7400 Analog I/O
- 7500 Industrial I/O
- 7600 Digital (TTL) I/O
- 7700 Memory
- 7800 Processors
- 7900 Utility (extenders, blanks, prototyping aids, etc.)

CMOS versions of many of the STD BUS cards are also offered. They are identified as the 70C00 Series (The 7000 and the 70C00 Series should not be used on the same bus.)

This section contains specifications common to the Series 7000 cards. These specifications, combined with the STD BUS specifications and the user's manuals for the individual cards, fully define each card. Configuring the hardware for a Series 7000 STD BUS system simply requires the defining of the memory size and the number and type of I/O lines needed for the application, together with the selection of the appropriate card rack and special cards. Mapping of the memory and I/O is preassigned, changes may be incorporated by moving jumper wires.





M AND N SERIES SINGLE & DUAL OUTPUT MODELS

- Low Noise
- Pi Input Filter
- Triple Fault Protection
- Regulation to 0.1%

The M and N Series consist of 15 single output and 10 dual output DC/DC converters that provide 10 watts total output power. Both series operate at efficiencies up to 71%, with 500 VDC isolation and only 1 mV RMS (40 mV P-P) output ripple and noise. All models are encapsulated in a compact 3 x 2.56 x .75 inch case.

Designed for maximum noise containment, the units feature a six-sided continuous package shield and transformer shield for EMI/RFI suppression, plus a Pi input filter to minimize reflected input ripple current. M Series single output models offer a number of fault protection features, including an internal thermal shutdown circuit designed to limit output current when case temperature exceeds a predetermined point. An internal overvoltage clamp is standard on M Series units.

10 Watt

ELECTRICAL SPECIFICATIONS

All Specifications Typical at Nominal Line, Full Load, and 25°C Unless Otherwise Noted.

OUTPUT SPECIFICATIONS

Voltage Accuracy	±1.0%, max.
Voltage Balance, —Output at Full Load (N Series Only)	±1.0%, max.
Load Regulation	See Table at Right
Line Regulation	See Table at Right
Ripple and Noise, 5 Hz to 20 MHz BW	1 mV RMS, max.
5 Hz to 20 MHz BW	40 mV P-P, max.
Average Voltage Temp. Coefficient	±0.01%/°C max.
Voltage Stability	±0.05%/24 hrs.
Transient Recovery Time to Within 0.5% of Final Value	
FL-NL, M Series	250 μsec., max.
FL-NL, N Series	150 μsec., max.
Short Circuit Protection	
M Series	Output to Common
N Series	Either Output to Output Common
Overvoltage Protection (M Series Only)	See Table Below

INPUT SPECIFICATIONS

Input Voltage Range	See Table Below
Input Filter	Pi Network

GENERAL SPECIFICATIONS

Efficiency, FL	See Table at Right
Isolation Voltage	>500 VDC
Isolation Resistance	>10⁹ Ohms
Switching Frequency	>20 KHz

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature Range	−25°C to +71°C
Derating, −25°C to +71°C	None Required
Storage Temperature Range	−40°C to +100°C
Case Temp. Rise Above Ambient	5°C/Watt Diss.
Internal Temp. Protection	Automatic Thermal Shutdown with Self-Resetting Output
Cooling	Free-Air Convection
EMI/RFI	Six-Sided Continuous Shield Transformer Shield

PHYSICAL SPECIFICATIONS

Dimensions	3.0 x 2.56 x .75 Inches (76 x 66 x 19 mm)
Weight	12 oz. (336 g.)
Case Material	Low Thermal Gradient Metal
Mating Socket	MS-X

INPUT VOLTAGE RANGES

NOMINAL	RANGE
5V	4.5-5.5V
12V	10-14.5V
24V	21-28V
28V	24-32V
48V	42-56V

OVERVOLTAGE RANGES (M SERIES)

OUTPUT	OVP SET
5V	6.8V
12V	15V
15V	18V

Other Input/Output Combinations Available—Consult Factory

Stevens-Arnold

TWO-YEAR WARRANTY

DC/DC Converters

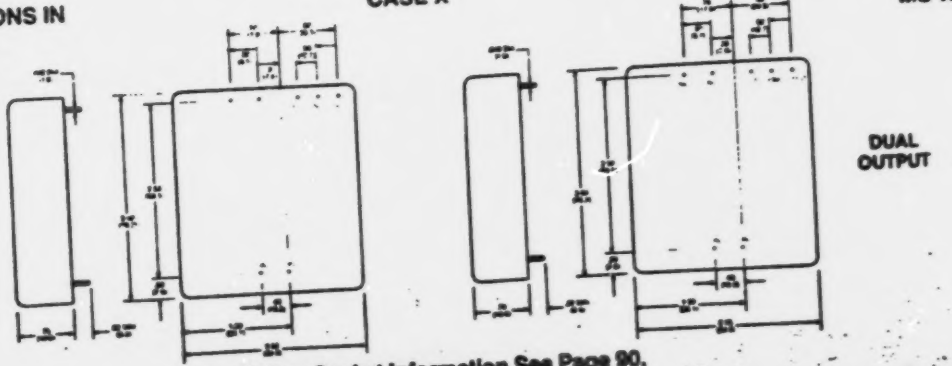
PACKAGED POWER

INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT CURRENT		% EFF	REGULATION		MODEL NUMBER	CASE
			NO LOAD	FULL LOAD		LINE	LOAD		
SINGLE OUTPUT									
5 VDC	5 VDC	2000 mA	400 mA	3100 mA	65	±0.2%	±0.2%	M05S05/2000X	X
	12 VDC	1000 mA	400 mA	3700 mA	65	±0.2%	±0.2%	M05S12/1000X	X
	15 VDC	670 mA	350 mA	3100 mA	65	±0.2%	±0.2%	M05S15/670X	X
12 VDC	5 VDC	2000 mA	80 mA	1350 mA	62	±0.2%	±0.2%	M12S05/2000X	X
	12 VDC	1000 mA	76 mA	1490 mA	67	±0.2%	±0.2%	M12S12/1000X	X
	15 VDC	670 mA	75 mA	1250 mA	67	±0.2%	±0.2%	M12S15/670X	X
24 VDC	5 VDC	2000 mA	35 mA	650 mA	64	±0.2%	±0.2%	M24S05/2000X	X
	12 VDC	1000 mA	35 mA	700 mA	71	±0.2%	±0.2%	M24S12/1000X	X
	15 VDC	670 mA	31 mA	600 mA	70	±0.2%	±0.2%	M24S15/670X	X
28 VDC	5 VDC	2000 mA	30 mA	530 mA	67	±0.2%	±0.2%	M28S05/2000X	X
	12 VDC	1000 mA	31 mA	635 mA	68	±0.2%	±0.2%	M28S12/1000X	X
	15 VDC	670 mA	30 mA	505 mA	71	±0.2%	±0.2%	M28S15/670X	X
48 VDC	5 VDC	2000 mA	25 mA	300 mA	69	±0.2%	±0.2%	M48S05/2000X	X
	12 VDC	1000 mA	25 mA	355 mA	70	±0.2%	±0.2%	M48S12/1000X	X
	15 VDC	670 mA	25 mA	300 mA	70	±0.2%	±0.2%	M48S15/670X	X
DUAL OUTPUT									
5 VDC	±12 VDC	±330 mA	500 mA	2700 mA	59	±0.1%	±0.1%	N05D12/330X	X
	±15 VDC	±330 mA	500 mA	3200 mA	62	±0.1%	±0.1%	N05D15/330X	X
12 VDC	±12 VDC	±330 mA	85 mA	1100 mA	60	±0.1%	±0.1%	N12D12/330X	X
	±15 VDC	±330 mA	85 mA	1300 mA	63	±0.1%	±0.1%	N12D15/330X	X
24 VDC	±12 VDC	±330 mA	37 mA	510 mA	65	±0.1%	±0.1%	N24D12/330X	X
	±15 VDC	±330 mA	35 mA	600 mA	69	±0.1%	±0.1%	N24D15/330X	X
28 VDC	±12 VDC	±330 mA	35 mA	450 mA	63	±0.1%	±0.1%	N28D12/330X	X
	±15 VDC	±330 mA	35 mA	525 mA	67	±0.1%	±0.1%	N28D15/330X	X
48 VDC	±12 VDC	±330 mA	20 mA	255 mA	65	±0.1%	±0.1%	N48D12/330X	X
	±15 VDC	±330 mA	25 mA	290 mA	71	±0.1%	±0.1%	N48D15/330X	X

ALL DIMENSIONS IN INCHES (MM)

CASE X

MATING SOCKET: MS-X



For Mating Socket Information See Page 90.

A.5 SPÉCIFICATIONS DES CONVERTISSEURS DC/DC

SEMICONDUCTOR CIRCUITS
Switch Mode Regulated DC/DC Converters

- SINGLE OUTPUTS TO 30 WATTS
- 2:1 INPUT RANGE
- CONVERTER SHUTDOWN INPUT PROTECTION

The UM, UMC Series are very efficient (to 80%) single output DC/DC converters that offer the versatility of a 2:1 input range.

The series offers input ranges of 9-18 Vdc, 18-36 Vdc and 35-70 Vdc and can withstand surges of 25, 60 and 100 V respectively for 12, 24 and 48 Vin models. The self-resetting shutdown, which occurs at 19 V, 38 V and 75 V, depending on model, protects the supply in the event of an input supply failure while input filtering holds reflected ripple to 30 mA Pk-Pk (max) to protect the input source from internally generated "spikes".

The UM, UMC Series offers single outputs of 5, 12 and 15 Vdc at from 1 A to 4 A. All outputs are free of chip damaging overshoot and are overcurrent protected by power foldback. Overvoltage protection is by automatic self-resetting crowbar. Thus, this series offers protection for both the input source and output load making it system safe for a variety of applications.

This series features input to output (I/O) isolation of 1500 Vdc and is available in both chassis mount (UMC) and P.C. mount (UM) versions by model designation.

Careful design techniques of this pulse width modulated forward converter series result in a low case temperature rise of less than 15°C above ambient, for all but the 30 watt models which have a rise of less than 25°C. This cool operation substantially increases the MTBF of the converter and nearby load circuitry.

Application Notes

The 2:1 input range makes the UM, UMC series ideal for use where the input source is poorly regulated. The worst situations involve industrial process control where raw 24 Vdc is bussed over long distances, therefore being subject to noise pickup and large inductive spikes caused by load changes.

Telecommunications applications operating from 48 V central office batteries are susceptible to wide voltage variations, due to battery charge and discharge cycles, as well as high noise conditions. The special features used in this converter allow the use of external transient suppression devices that do not draw any current within the operating specifications of the converter. (See catalog page 47, for a discussion of input transient suppression.)

General Specifications

Input Reflected Ripple
30 mA pk-pk (max)

Output Voltage Tolerance
± 2% Fixed

Regulation (line/load)
0.1/0.1%

Ripple & Noise
7 mV (VRMS). Greater of 50 mV pk-pk or 1% of Vout (Vpk-pk)

Operating Temperature Range
– 25°C to + 71°C (no derating)

Storage Temperature Range
– 40°C to + 85°C

Input to Output Isolation
Voltage 1500 Vdc

Temperature Coefficient
0.02%/°C (typ)

Overcurrent Protection
Power Foldback

Overvoltage Protection
Automatic self-resetting crowbar

Input Protection
(Converter Shutdown)

9-18 V Rated Input
25 V sustained, shutdown set at 19 V

18-36 V Rated Input
60 V sustained, shutdown set at 38 V

35-70 V Rated Input
100 V sustained, shutdown set at 75 V

Switching Frequency
33 kHz (typ)

Startup Time
70 ms (typ)

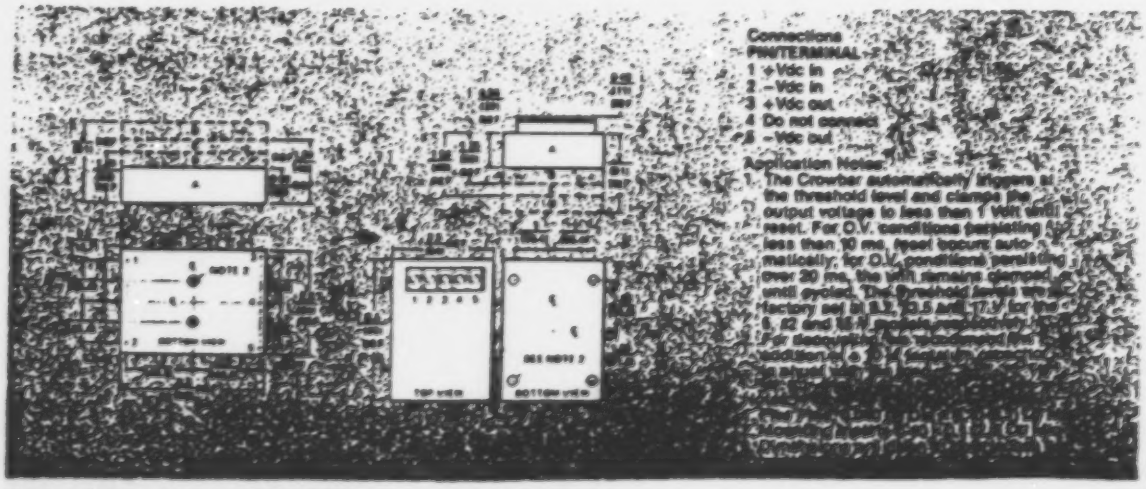
SEMICONDUCTOR CIRCUITS, INC.

Ordering Information

Input Voltage Range (Vdc)	Output Voltage (Vdc)	Output Current (Vdc)	Efficiency (%)	Pkg. (Fig.)	Model Number	Options**
9-18	5V	3000	70-80	1-C 2-D	UM11-300-12 • UMC11-300-12 •	
18-36			70-80	1-C 2-D	UM11-300-24 • UMC11-300-24 •	
35-70			70-80	1-C 2-D	UM11-300-48 • UMC11-300-48 •	
18-36		4000	70-80	1-D 2-D	UM11-400-24 • UMC11-400-24 •	
35-70			70-80	1-D 2-D	UM11-400-48 • UMC11-400-48 •	
9-18	12V	1000	70-80	1-C 2-D	UM12-100-12 • UMC12-100-12 •	
18-36			70-80	1-C 2-D	UM12-100-24 • UMC12-100-24 •	
35-70			70-80	1-C 2-D	UM12-100-48 • UMC12-100-48 •	
35-70		2000	70-80	1-D 2-D	UM12-200-48 • UMC12-200-48 •	
9-18	15V	1000	70-80	1-C 2-D	UM13-100-12 • UMC13-100-12 •	
18-36			70-80	1-C 2-D	UM13-100-24 • UMC13-100-24 •	
35-70			70-80	1-C 2-D	UM13-100-48 • UMC13-100-48 •	
35-70		2000	70-80	1-D 2-D	UM13-200-48 • UMC13-200-48 •	

*Other versions available, please consult factory
**For complete option description, refer to catalogue page 43
•Available from stock; contact local distributor, area rep or factory.
Socket Information: Standard UM, UMC use socket P/N #100013
(For socket dimensional information refer to catalogue page 42.)

Dimensions and Connections



Testing: See Catalog pages 45 and 46 for proper testing procedures.
Specifications Subject to Change Without Notice.

APPENDICE B
RADIOMÈTRE

CRIQ

COM DEV

DRAFT

DESIGN, OPERATION AND MAINTENANCE

MANUAL

FRONT END ASSEMBLY
CRIQ RADIOMETER SENSOR

SUPPLIED BY COM DEV LTD
155 SHELDON DRIVE
CAMBRIDGE, ONTARIO

COM DEV

TABLE OF CONTENTS

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2.0	PARTS LIST	2
3.0	OPERATION	9
4.0	MAINTENANCE	10

LIST OF FIGURES

FIGURE		PAGE
FIGURE 1	PHOTOGRAPH OF FRONT END ASSEMBLY	3
FIGURE 2:	BLOCK DIAGRAM OF FRONT END ASSEMBLY	4

COM DEV

1.0 INTRODUCTION

This manual describes the design, operation and maintenance procedure of the Front End Assembly for the CRIQ Radiometer Sensor. The Front End Assembly was supplied by COM DEV Ltd (formerly Antech Antenna Technologies Ltd), Cambridge, Ontario.

COM DEV

2.0 PARTS LIST

The following components are assembled to form the Front End Assembly. This assembly is illustrated in Figure 1. A block diagram is provided in Figure 2.

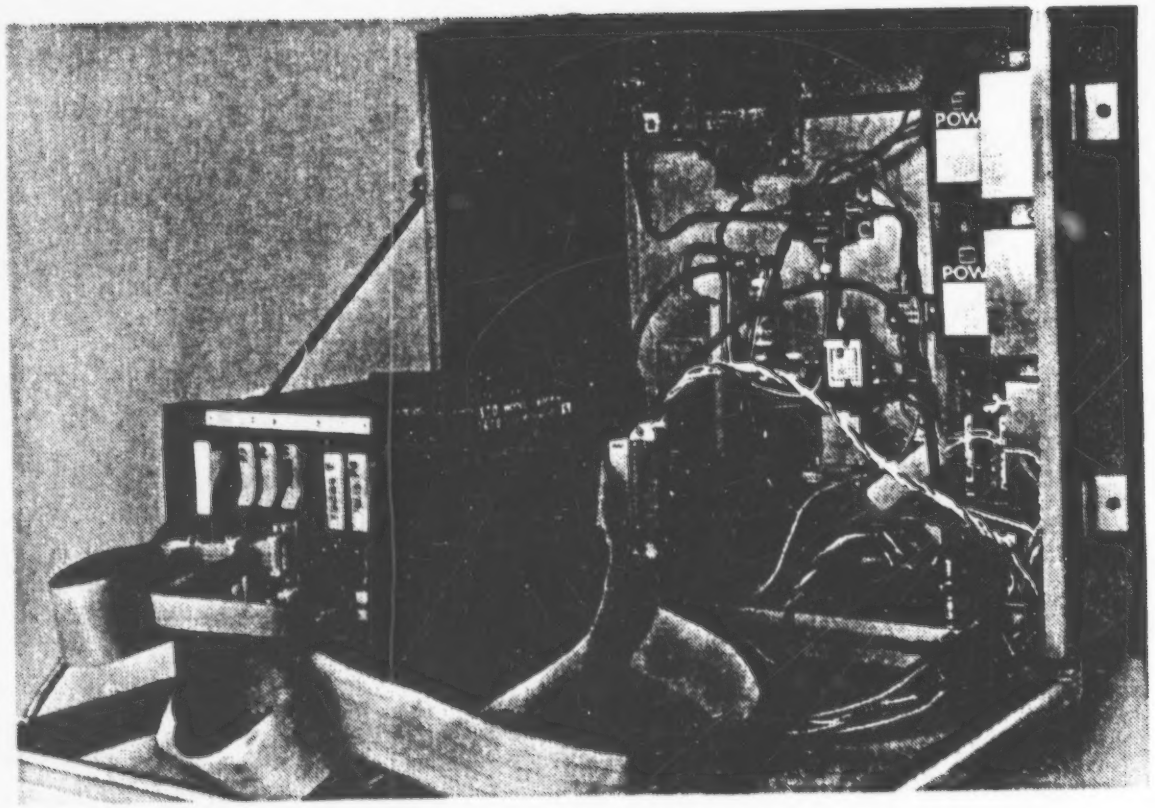


FIGURE 1: PHOTOGRAPH OF FRONT END ASSEMBLY

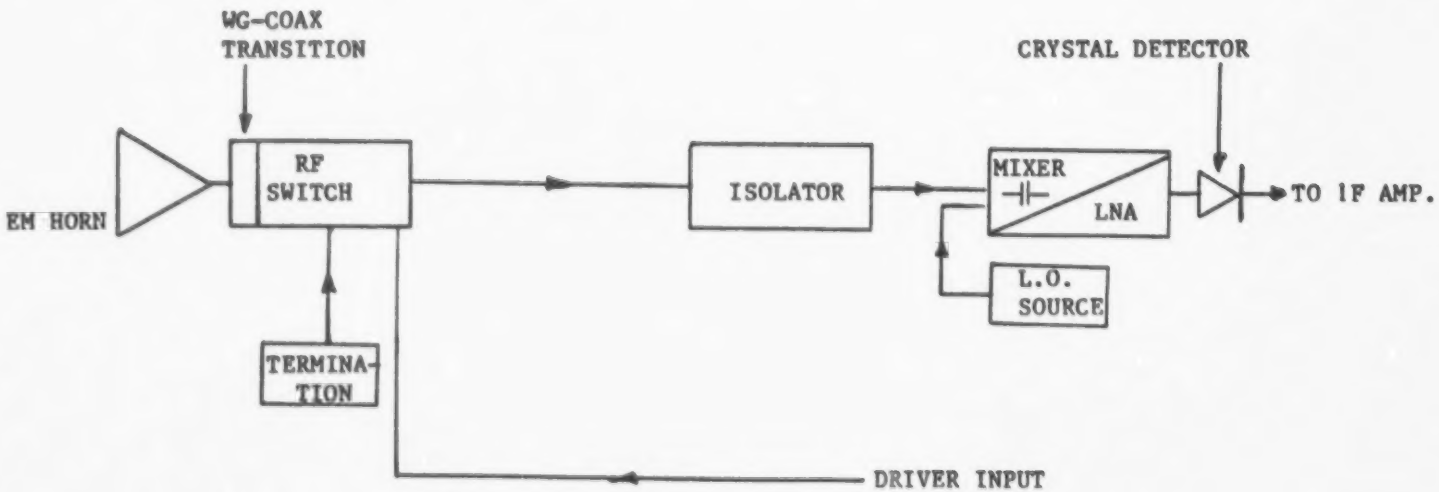


FIGURE 2: BLOCK DIAGRAM FRONT END ASSEMBLY

COM DEV

SCHEDULE OF COMPONENT
FRONT END ASSEMBLY

ITEM	QTY	DESCRIPTION	MANUFACTURER	MODEL
1	1	Sector Beam Electromagnetic Horn and Cover and Base Plate	COM DEV	ANT-CRQ-O
2	1	RF Switch	General Microwave	FS77012-218
3	1	Waveguide-Coax Transition	Maury Microwave	X230B
4	1	Isolator	Junction Devices	3X30I
5	1	Mixer	RHG	DMX8-12
6	1	Cavity Stabilized Source	Frequency Sources	FS-2200
7	1	Low Noise Amplifier	Trontech	W2G10B-4
8	1	Crystal Detector	Micronetics	DM12.4
9	1	Termination	Omni-Spectra	20016100-00
10	1	Set RF Cable Assemblies	R.F. Microwave	-
11	1	D.C. Block	Midwest Microwave	3510

COM DEV

The following summarizes individual component specifications to aid in selection of alternate supplies in the event of failure of any component.

1. Electromagnetic Horn

Frequency	10.025 GHz
E-Plane Beamwidth	70°
H-Plane Beamwidth	41.2°
VSWR	1.5

2. RF Switch

Frequency	8 - 12.4 GHz
Min. Isolation	55 dB
Max. Insertion Loss	1.75 dB
VSWR	1.75

3. Waveguide-Coax Transition

Frequency	8.2 - 12.4 GHz
Waveguide	WR90
VSWR	1.25

4. Isolator

Frequency	8.0 - 12.0 GHz
Isolation	20 dB

COM DEV

Insertion Loss	0.4 dB
VSWR	1.22

5. Mixer

Frequency	8.0 - 12.0 GHz
N.F.	9.0 dB typical
	10.0 dB Max.

6. Cavity Stabilized Source

Frequency	5.5 - 18.0 GHz
Mechanical Tuning Range	6%
Power Output	10 mW
DC Power	+15V 500-750 mA
Harmonic Suppression	-25 dB

7. Low Noise Amplifier

Frequency	.01 - 2 GHz
Noise Figure	3.0 dB Typ.
	3.5 dB Max.
Gain	50 dB
Flatness	I 0.6 dB
1 dB Gain Compression	0 dB
Interpret Point for 1 dB Comp.	+12 dBm
Input Power	+15 V, 30mA

COM DEV

8. Crystal Detector

Frequency	0.01 - 12.4 GHz
Frequency Response	±0.5 dB/octave
Low Level Sensitivity	0.4 mV/µW
High Level Sensitivity	100mV/0.35 mW
Output Polarity	Negative
VSWR	1.4

9. Termination

Frequency	0.01 - 12 GHz
VSWR	1.1

10. D.C. Block

Frequency	250MHz - 18,5GHz
VSWR	1,35
Max. Insertion loss	0,5dB

3.0 OPERATION

The front end assembly serves as the input circuit for the CRIQ Radiometer system. Noise-like radiometry signals are received by the electromagnetic horn when the RF switch is in the A condition. The amplitude of these signals is a function of the noise temperature of the surrounding environment. The noise temperature will vary depending on the nature of the objects entering the beam of the EM horn. The waveguide port of the horn is converted at this point to coaxial line.

In the B position of the switch, the circuit is connected to a termination which is at the ambient temperature. In most cases, this termination acts as a noise source at ambient temperature in the range of 270K ± 30 K. This is considerably hotter than the temperature sensed by the EM horn when the cold sky noise is reflected by a good reflector into the radiometer.

The RF switch is driven by an external driver circuit at a rate of 1 kHz. The switched signals then pass through an isolator which maintains constant impedance condition, irrespective of switching state, for proper operation of the mixer. After mixing, signals are amplified in the LNA and detected.

COM DEV

4.0 MAINTENANCE

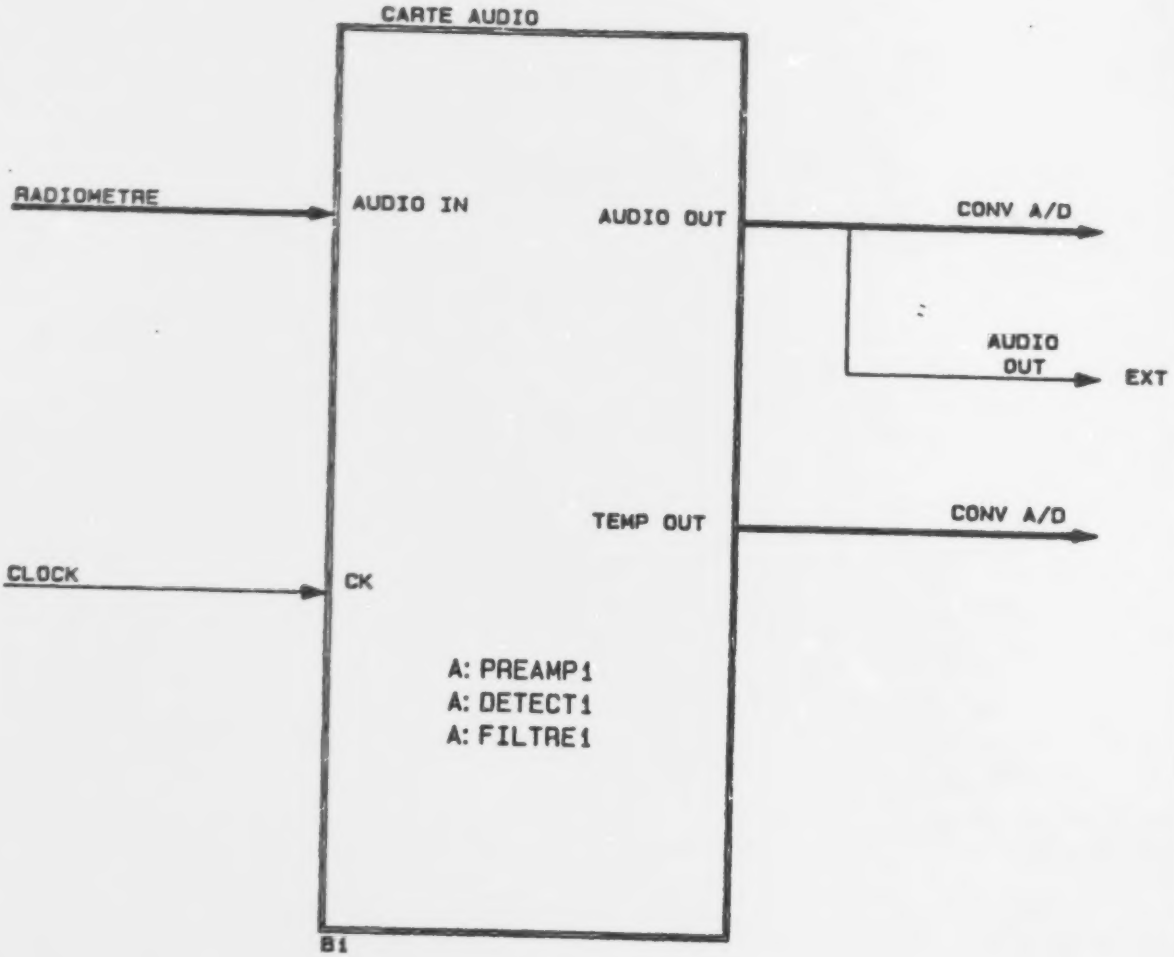
The assembly is essentially maintenance free under normal operating conditions. All components are easily removable with the exception of the EM horn. This is a highly reliable component and will not change characteristics unless physically damaged.

Should a failure occur, normal removal and check-out of each component will suffice to identify the failure. Replacement of the component is recommended.

In replacing components, extreme care must be taken to avoid damage to connectors. Connectors should be thoroughly inspected for dirt, pin alignment and protrusion before rejoining.

The assembly should be inspected for cleanliness during routine maintenance of the system.

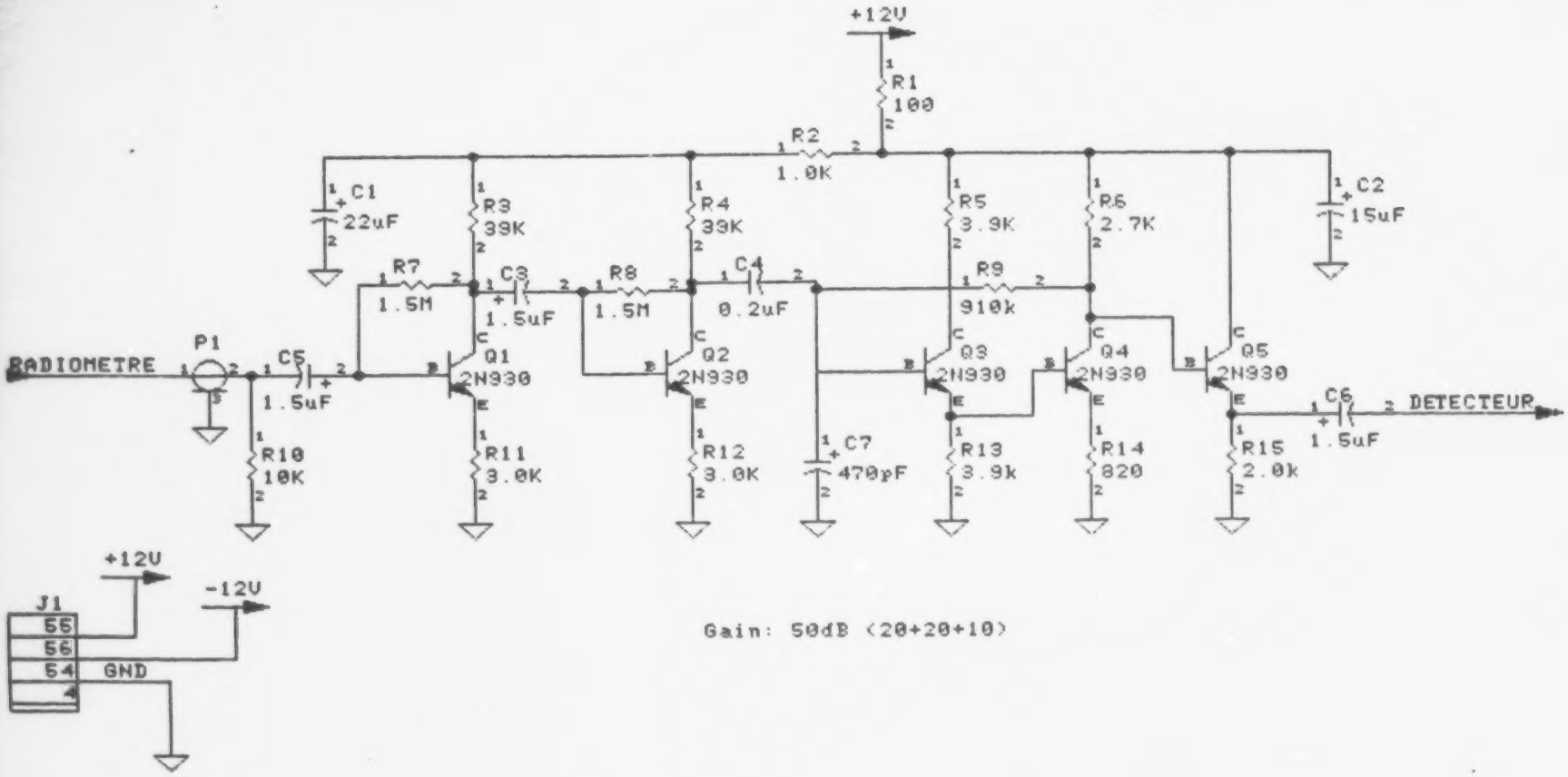
APPENDICE C
CARTE AUDIO



REV.	ZONE	DESCRIPTION	No. ADC	DATE	APP.

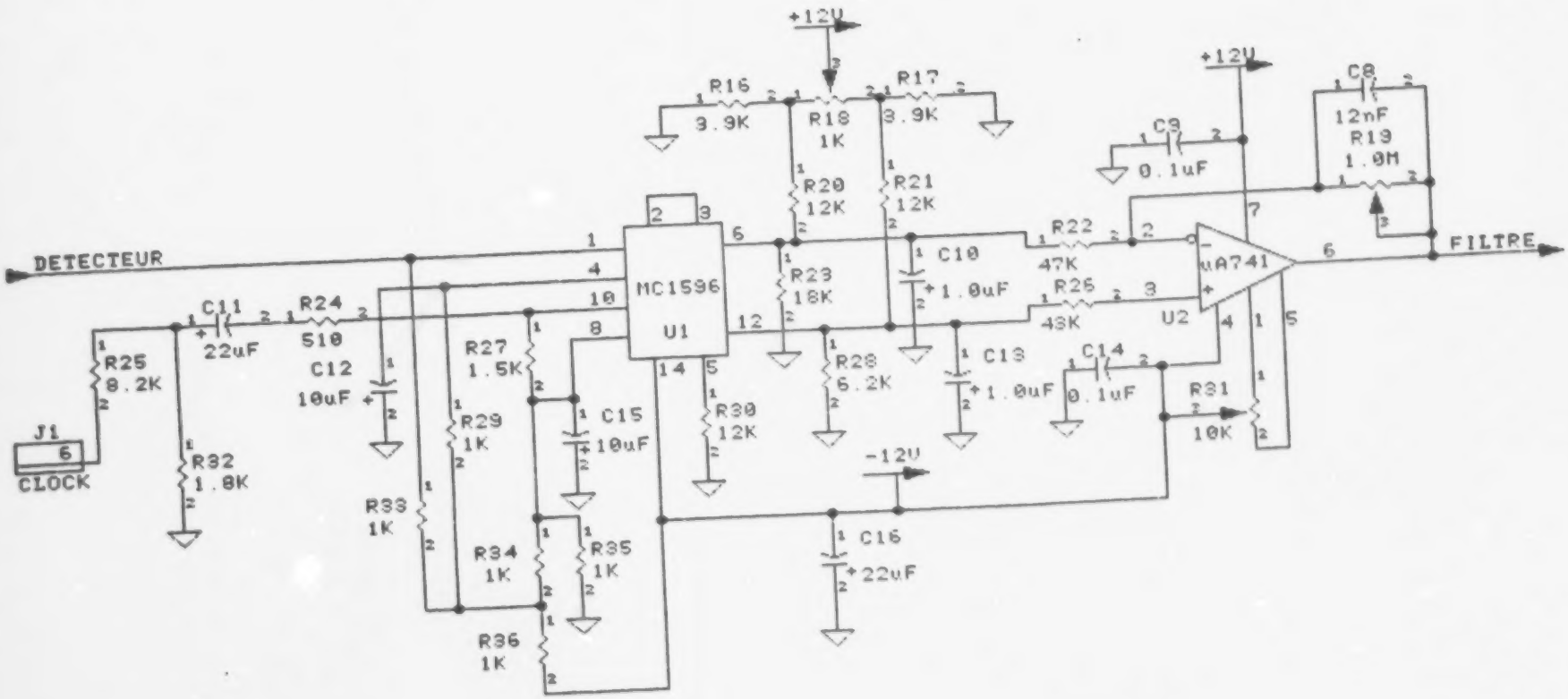
ENSEMBLE SUIVANT		PROJET	CRIQ CENTRE DE RECHERCHE INDUSTRIELLE DU QUÉBEC
TOLERANCES NON SPEC.		SIGNATURES / DATES	
ANGLES	±	DESSINE	TITRE: CARTE AUDIO
UNITES	±	VERIFIE	A4 NO. DESSIN
DECIMALES	.X ± / .XX ±	APPROUVE	ECHELLE / EDITION / FEUILLE 1 DE 4
ECHELLE NON GARANTIE			

Imprimé le 11 85

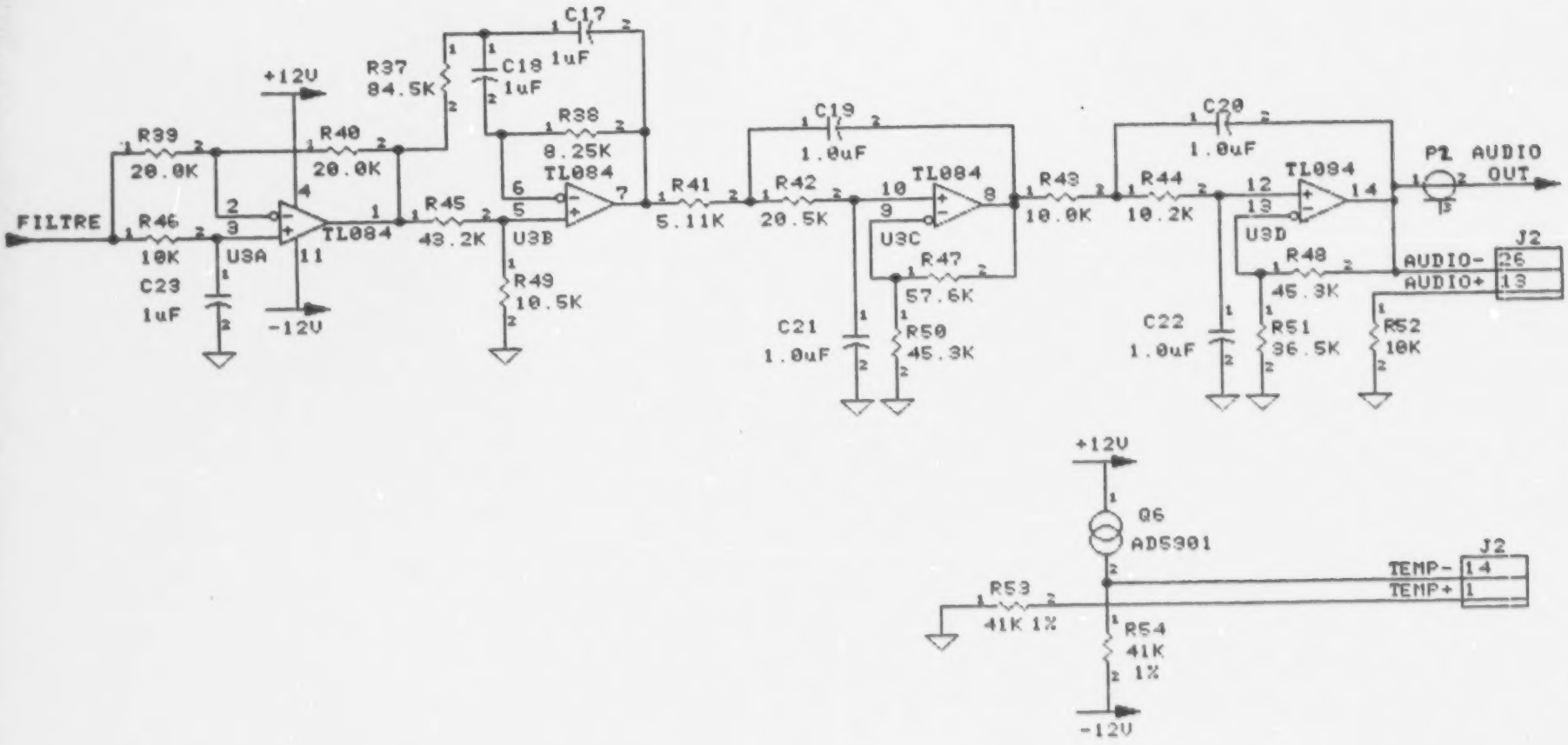


Gain: 50dB (20+20+10)

PREAMP
08/04/81



DETECT
08/04/86


FILTRE
R46
10K
C23
1uF
U3A
TL084
+12V
-12V
R39
20.0K
R40
20.0K
R37
84.5K
C17
C18 1uF
1uF
R38
8.25K
R45
43.2K
U3B
TL084
R49
10.5K
R41
5.11K
C19
1.0uF
R42
20.5K
U3C
TL084
R47
57.6K
C21
1.0uF
R50
45.3K
R43
10.0K
C20
1.0uF
R44
10.2K
U3D
TL084
R48
45.3K
C22
1.0uF
R51
36.5K
R52
10K
P1 AUDIO OUT
J2
AUDIO-
AUDIO+
26
13
+12V
Q6
ADS301
R53
41K 1%
R54
41K
1%
-12V
J2
TEMP-
TEMP+
14
1
FILTRE
09/04/'86

APPENDICE D

CONVERTISSEUR ANALOGUE A DIGITAL

(LPM - A/D)

CRIQ

wintech
SYSTEMS INC.

OPERATIONS MANUAL
LPM-A/D

WINTECH SYSTEMS, INC. reserves the right to make changes in the circuitry and specifications at any time without notice.

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WINTECH SYSTEMS, INC. • Box 121361 • Arlington, Texas 76012 • 817-274-7553

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		PARTS LIST	
		WARRANTY AND REPAIR INFORMATION	

SECTION 1
GENERAL INFORMATION

1.1 FEATURES

* STD BUS COMPATIBLE
* 12 BIT LOW POWER A/D
* EXTENDED TEMPERATURE OPERATION -25 C TO +85 C
* 16 SINGLE ENDED OR 8 DIFFERNTIAL CHANNELS
* INTERRUPT ON CONVERSION
* 5 INPUT VOLTAGE RANGES
* OPTIONAL DC/DC CONVERTOR FOR +5V OPERATION

1.2 GENERAL DESCRIPTION

1.2.1 The LPM-A/D is a low power 12 bit analog to digital converter board designed for the STD BUS. The LPM-A/D offers the user 16 single ended or 8 differential channels with five jumper selectable input voltage ranges. The LPM-A/D can be operated from +/- 12 VDC or +/- 15 VDC supplied from the STD BUS or from +5 VDC only with an optional on board DC/DC converter. (NOTE: For +/- 12 VDC operation, the input range is limited to +/- 5 VDC) Lower input voltage ranges can be accomodated by installing a single resistor to increase the gain of the instrumentation amplifier.

1.2.2 The LPM-A/D is designed with the Datel ADC-HC12BMR analog to digital convertor for low power and extended temperature operation. The ADC-HC12BMR is a 12 bit CMOS ADC that has a 305 us conversion time. The ADC-HC12 produces straight binary for unipolar voltages, and offset binary for bipolar voltages. In addition, the MSB can be complemented to produce 2's complement.

1.2.3 The 16 channels for singled ended operation or 8 channels for differential operation is implemented by the use of two 8 channel CMOS switches. These switches can withstand +/- 20 V with the power off, or +/- 32 V with the power on. Digital inputs for selecting a particular channel are controlled by a 4 bit latch that holds the channel number for conversion. A new conversion is begun each time that a new channel number is written into the latch.

1.2.4 The input multiplexers feed the instrumentation amplifier. The LPM-A/D uses the Burr-Brown INA-101 monlithic instrumentation amplifier for high input impedance and common mode rejection. The input of the instrumentation amplifier can be jumpered for single ended or differential operation.

1.2.5 The output of the ADC is controlled by I/O ports that are interfaced to the STD BUS. One write only port is used to output the channel number and begin the conversion. Two read ports are used to allow the 12 bits from the ADC, and status information to be read. A complete conversion can be detected by polling the BUSY flag or by enabling interrupts on the LPM-A/D. When using

the interrupt method, the LPM-CPU interrupts must be enabled, and in the interrupt mode 1 configuration. When the conversion is complete, the LPM-A/D will interrupt the LPM-CPU and the data can then be read out by the use of an interrupt service routine. The interrupt is cleared on the LPM-A/D by reading the data.

1.3 SPECIFICATIONS

ANALOG INPUT
Number of Channels 16 single ended or eight differential
Input Impedance 100 megohm
Input Overvoltage +/- 35V (+/- 20V with power off)
Input Ranges +/- 2.5V,+/- 5V, 0-5V with +/- 12V supplies
+/- 2.5V, +/-5V, +/- 10V, 0-5V, 0-10V with +/- 15V
Coding, unipolar straight binary
Coding, bipolar offset binary, 2's complement
Resolution 12 bits
Nonlinearity +/- 1/2 LSB
Differential Nonlinearity +/- 1/2 LSB
Gain Error Adjustable to zero
Offset or Zero Error Adjustable to zero
Accuracy +/- .03 % FSR
Conversion Time 365 us

INTERFACE
All address, data, and control lines are CMOS/STD BUS compatible

CONNECTOR
56 pin dual 0.125 inch centers

POWER REQUIREMENTS
Without DC to DC Convertor
+5 VDC +/- 10% at 5 ma.
+12/15 VDC +/- 5% 20 ma.
-12/15 VDC +/- 5% 15 ma.

With DC to DC Convertor
+5 VDC +/- 10% at 200 ma.

OPERATING TEMPERATURE
-25 C to +85 C (Extended temperature range)

CARD DIMENSIONS
Height 6.5 inches
Width 4.48 inches
Thickness .50 inches

SECTION 2
USER OPTIONS

2.1 I/O ADDRESS DECODER

2.1.1 The LPM-A/D is an I/O mapped device, and uses one write only I/O port and two read only ports. A jumper selectable address decoder is used so that several I/O boards can be used in a system without data bus contention problems. The LPM-A/D can be strapped for sixteen different I/O addresses by the use of jumper block J6. These I/O addresses are shown in table 2-1 with the strapping for J6. See figure 2-4 for the LPM-A/D I/O map.

TABLE 2-1
I/O ADDRESS DECODER STRAPPING

HEX	0-2	4-6	8-A	C-E	10-12	14-16
	1o—o2 3o—o4 5o—o6 7o—o8	1o—o2 3o—o4 5o—o6 7o o8	1o—o2 3o—o4 5o o6 7o—o8	1o—o2 3o—o4 5o o6 7o o8	1o—o2 3o o4 5o—o6 7o—o8	1o—o2 3o o4 5o—o6 7o o8

HEX	18-1A	1C-1C	20-22	24-26	28-2A	2C-2E
	1o—o2 3o o4 5o o6 7o—o8	1o—o2 3o o4 5o o6 7o o8	1o o2 3o—o4 5o—o6 7o—o8	1o o2 3o—o4 5o—o6 7o o8	1o o2 3o—o4 5o o6 7o—o8	1o o2 3o—o4 5o o6 7o o8

HEX	30-32	34-36	38-3A	3C-3E
	1o o2 3o o4 5o—o6 7o—o8	1o o2 3o o4 5o—o6 7o o8	1o o2 3o o4 5o o6 7o—o8	1o o2 3o o4 5o o6 7o o8

NOTE: ADDRESS BITS A0,A1,A6, AND A7 ARE DECODED ON THE BOARD.

2.2 ANALOG INPUT CONNECTOR PIN OUT

2.2.1 The analog inputs to the LPM-A/D are made through connector J1 located at the top of the board. Table 2-2 shows the pin out for the 16 single ended channels and the eight differential channels.

TABLE 2-2
J1 PIN OUT FOR SINGLE ENDED OR DIFFERENTIAL OPERATION

J1

DIFFERENTIAL	SINGLE ENDED	PIN #		SINGLE ENDED	DIFFERENTIAL
CHAN 0 (+)	CHAN 0	1	14	CHAN 8	CHAN 0 (-)
CHAN 1 (+)	CHAN 1	2	15	CHAN 9	CHAN 1 (-)
ANALOG GROUND		3	16	ANALOG GROUND	
CHAN 2 (+)	CHAN 2	4	17	CHAN 10	CHAN 2 (-)
ANALOG GROUND		5	18	ANALOG GROUND	
CHAN 3 (+)	CHAN 3	6	19	CHAN 11	CHAN 3 (-)
ANALOG GROUND		7	20	ANALOG GROUND	
CHAN 4 (+)	CHAN 4	8	21	CHAN 12	CHAN 4 (-)
ANALOG GROUND		9	22	ANALOG GROUND	
CHAN 5 (+)	CHAN 5	10	23	CHAN 13	CHAN 5 (-)
ANALOG GROUND		11	24	ANALOG GROUND	
CHAN 6 (+)	CHAN 6	12	25	CHAN 14	CHAN 6 (-)
CHAN 7 (+)	CHAN 7	13	26	CHAN 15	CHAN 7 (-)

2.3 SINGLE ENDED AND DIFFERENTIAL INPUT CONFIGURATIONS

2.3.1 The LPM-A/D can be configured for single ended or differential operation. The singled ended mode of operation allows the maximum number of inputs channels (16), while the differential mode of operation only allows eight. The advantage of the differential mode is that it offers the highest noise rejection and common mode rejection ratio (CMMR) for low level data acquistion applications. Figure 2-1 shows the strapping for jumper blocks J2 and J3 for single ended operation. Figure 2-2 shows the strapping for differential operation.

FIGURE 2-1
J2,J3 STRAPPING FOR SINGLE ENDED OPERATION

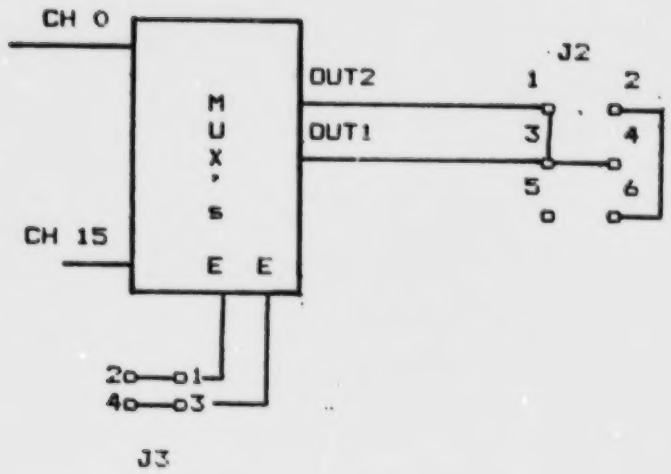
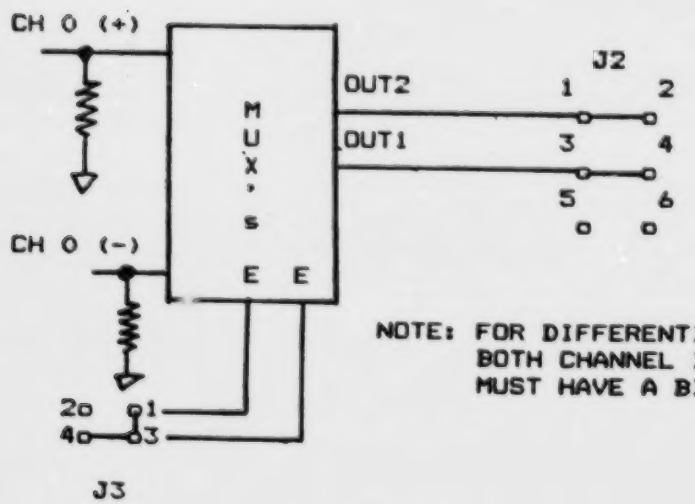


FIGURE 2-2
J2,J3 STRAPPING FOR DIFFERENTIAL OPERATION

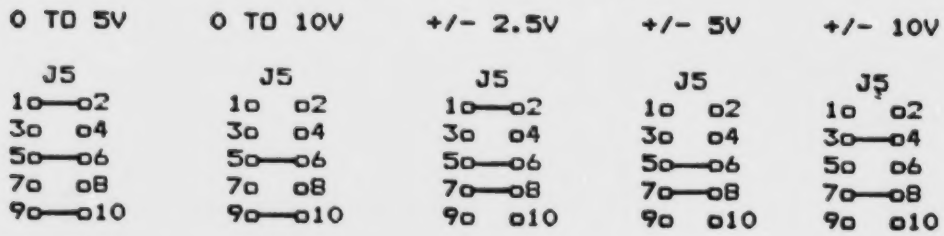


NOTE: FOR DIFFERENTIAL OPERATION,
BOTH CHANNEL INPUTS (+ AND -)
MUST HAVE A BIAS RETURN PATH!

2.4 INPUT RANGES

2.4.1 The LPM-A/D has five different input voltage ranges controlled by jumper block J5. Figure 2-3 shows the strapping for J5 vs the input voltage ranges. IMPORTANT NOTE: FOR INPUT VOLTAGE RANGES ABOVE 5 VOLTS, THE LPM-A/D MUST BE OPERATED WITH +/- 15 VDC SUPPLIES, OTHERWISE NON LINEAR OPERATION WILL RESULT.

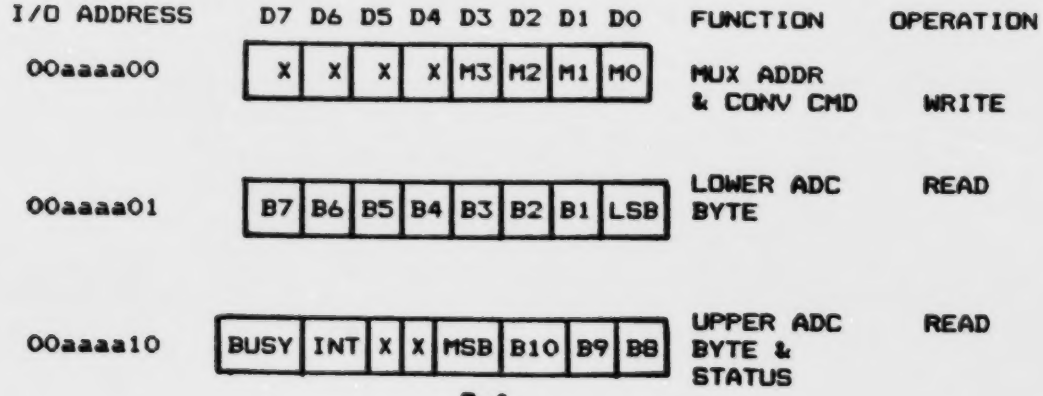
FIGURE 2-3
J5 INPUT VOLTAGE JUMPERS



2.5 SOFTWARE INTERFACE

2.5.1 The LPM-A/D is very simple to use. For example, assume that the LPM-A/D is strapped for I/O addresses 0-2 HEX, and single ended operation. To begin a conversion, channel number is loaded into the accumlator (A Register) and output to I/O port located at 0 HEX. This will cause the multiplexers to switch to channel 0, the BUSY bit located in input port bit 7 (MSB) to be set high indicating that a conversion is in progress. Approximately 350 us later, the BUSY bit will be reset indicating that the conversion is complete, and data can be read out from input ports 1 and 2. Input port 1 contains the least significant byte and the lower four bits of input port 2 contains the most significant four bits. Figure 2-4 shows the I/O port map for the previous example.

FIGURE 2-4
I/O PORT MAP FOR LPM-A/D



NOTES: 1. I/O address bits "aaaa" are programmable by the use of jumper block J6.

2. "X" bits are don't cares.

3. Busy bit is a "1" while a conversion is in progress and a "0" when finished.

4. The INT bit is set to a "1" when a conversion is completed, and will remain set until the lower ADC byte is read. The INT bit can be used by an interrupt service routine to determone if the LPM-A/D generated an interrupt to the LPM-CPU card.

5. Writing the multiplexer number to I/O port address 00aaaa00 will set the input channel and start a conversion.

6. A SYSTEM RESET will clear BUSY and INT.

2.5.2 The LPM-A/D is capable of generating an interrupt on the completion of a conversion cycle. The interrupt for the LPM-A/D is enabled by jumper block J7. See figure 2-5 below. At the end of a conversion cycle, the LPM-A/D will set the INT bit, and if enabled by J7, will activate the INTRQ line on the STD BUS. Both the INT bit in the status register and the INTRQ line on the STD BUS will remain active until data is read from the lower ADC input port. The INT bit in the status register can be used by an interrupt service routine to determine if the LPM-A/D generated an interrupt. See flowchart in figure 2-7 for interrupt service routine.

FIGURE 2-5
INTERRUPTS

INTERRUPTS ENABLED	INTERRUPTS DISABLED
J7	J7
o—o	o o

2.5.3 Figure 2-6 shows a flowchart for a "polled mode" software interface while figure 2-7 shows an "interrupt mode" interface for analog to digital conversion using the LPM-A/D.

FIGURE 2-6
LPM-A/D POLLED MODE FOR A/D CONVERSION

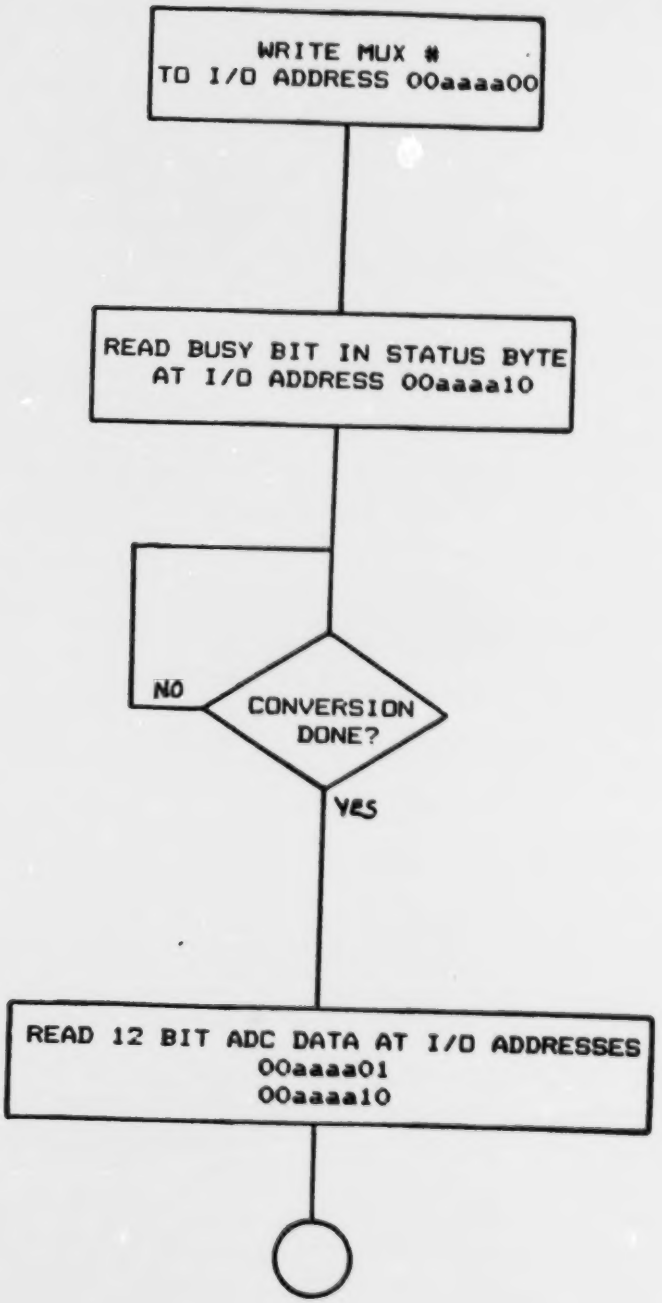
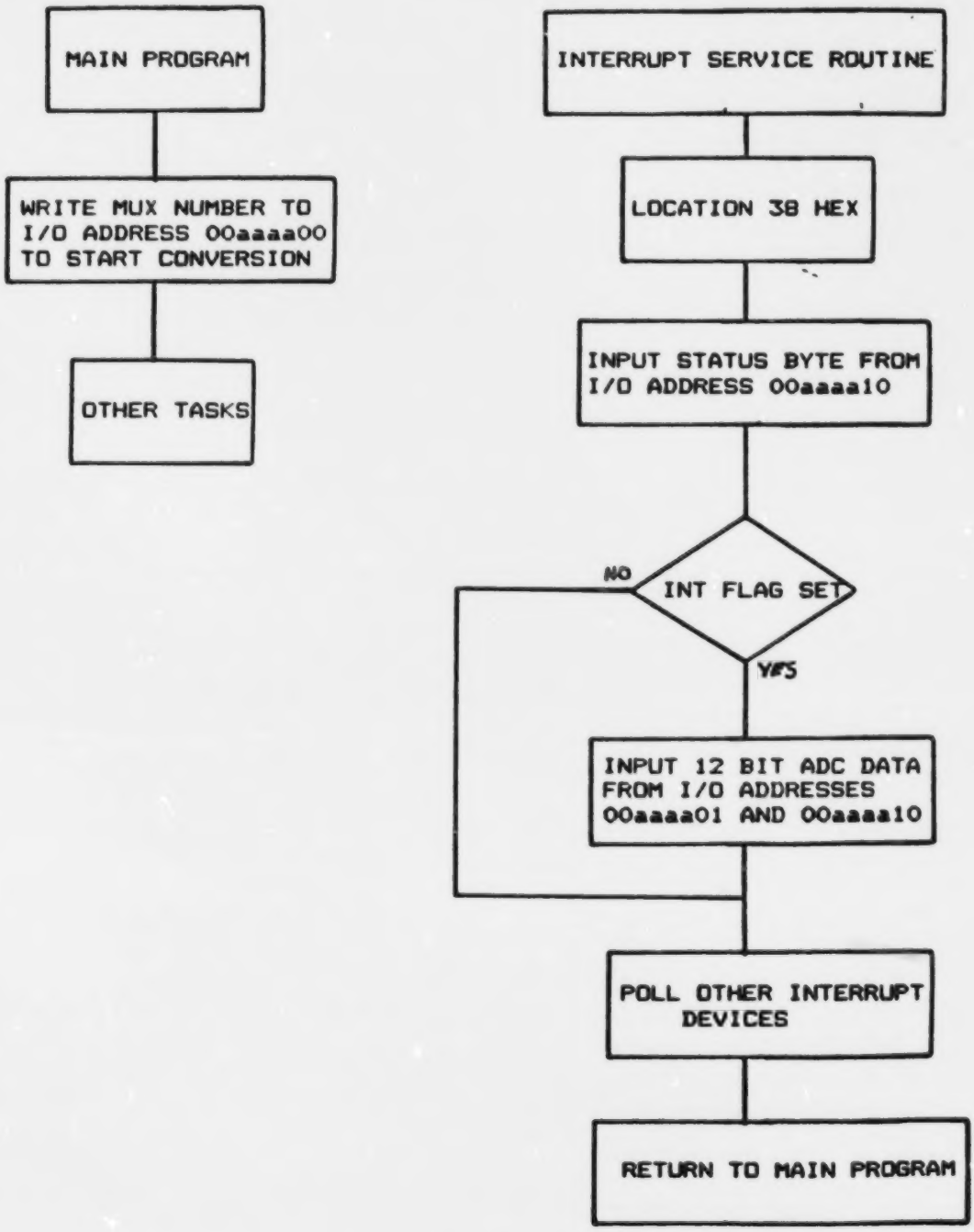


FIGURE 2-7
FLOWCHART FOR INTERRUPT MODE



2.6 CALIBRATION PROCEDURES

2.6.1 The LPM-A/D is calibrated at the factory for the 0-5V range of operation. When switching to another input range, a slight adjustment may be necessary. The following procedure is given calibrate the LPM-A/D for any input range. Figure 2-8 shows the output coding for the various input ranges. NOTE: TRIMPOT R4 IS USED TO ZERO THE SAMPLE AND HOLD AMPLIFIER AND SHOULD NOT BE HAVE TO BE ADJUSTED.

CALIBRATION PROCEDURE

1. Select the desired input voltage range as shown in section 2.4. Use one of the routines as described section 2.5, software interface to start and readout a conversion.

2. ZERO AND OFFSET ADJUSTMENT. (TRIMPOT R5)
Apply a voltage source between the selected analog channel and ground. Adjust the output of the voltage source to +1/2 LSB. Adjust the zero trimming potentiometer R5 so that the output code flickers equally between 000 HEX and 001 HEX for uniploar operation and 800 HEX and 801 HEX for the bipolar mode.

3. FULL SCALE ADJUSTMENT (TRIMPOT R6)
Change the output of the voltage source for +FS-1 1/2 LSB. Adjust the gain trimming potentiometer R6 so that the output code flickers equally between FFE HEX and FFF HEX.

FIGURE 2-8
OUTPUT CODING

INPUT VOLTAGE RANGE				CODING	
	UNIPOLAR			STRAIGHT BINARY	
	0 TO 10V	0 TO +5V		MSB	LSB
+FS-1 LSB	+9.9976	+4.9988		1111 1111 1111	
+1/2 FS	+5.0000	+2.5000		1000 0000 0000	
+1 LSB	+0.0024	+0.0012		0000 0000 0001	
ZERO	0.0000	0.0000		0000 0000 0000	
	BIPOLAR			OFFSET BINARY*	
	+/- 10V	+/- 5V	+/- 2.5V	MSB	LSB
+FS-1 LSB	+9.9951	+4.9976	+2.4988	1111 1111 1111	
+1/2 FS	+5.0000	+2.5000	+1.2500	1100 0000 0000	
+1 LSB	+0.0049	+0.0024	+0.0012	1000 0000 0001	
ZERO	0.0000	0.0000	0.0000	1000 0000 0000	
-FS-1 LSB	-9.9951	-4.9976	-2.4988	0000 0000 0001	
-FS	-10.0000	-5.0000	-2.5000	0000 0000 0000	

* FOR 2's COMPLEMENT, CONNECT J4 1-2, DISCONNECT J4 3-4

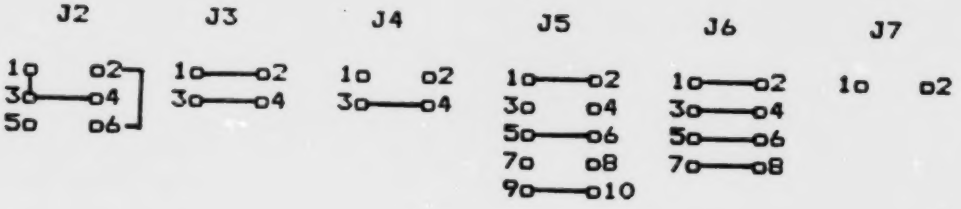
2.7 EXAMPLES

2.7.1 This section is provided to give some common application examples of the LPM-A/D.

EXAMPLE #1

Configuration:

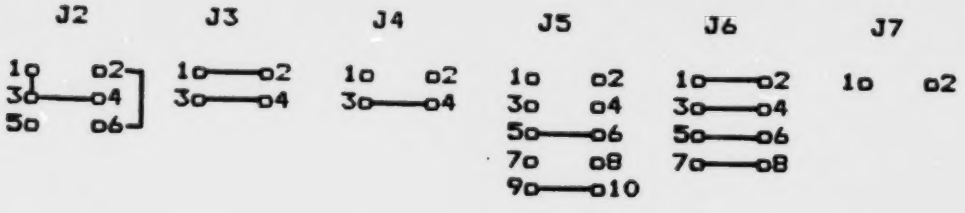
Number of input channels: 16 single ended
Input voltage range: 0-5V
I/O address: 0-2 HEX



EXAMPLE #2

Configuration:

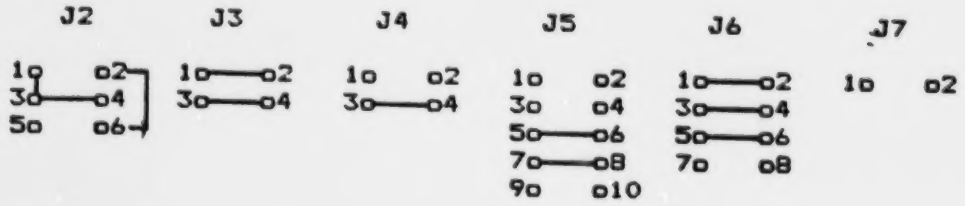
Number of input channels: 16 single ended
Input voltage range: 0-10V (REQUIRES +/- 15 VDC SUPPLIES)
I/O address: 0-2 HEX



EXAMPLE #3

Configuration:

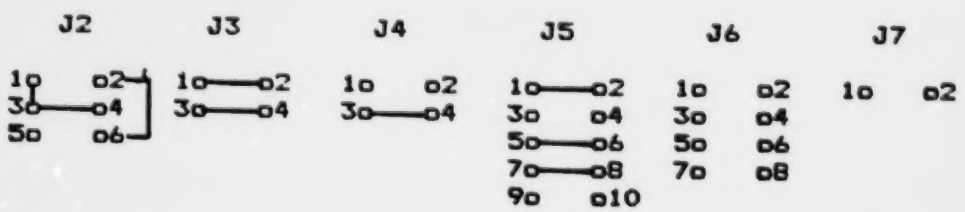
Number of input channels: 16 single ended
Input voltage range: +/- 5 V
I/O address: 4-6 HEX



EXAMPLE #4

Configuration:

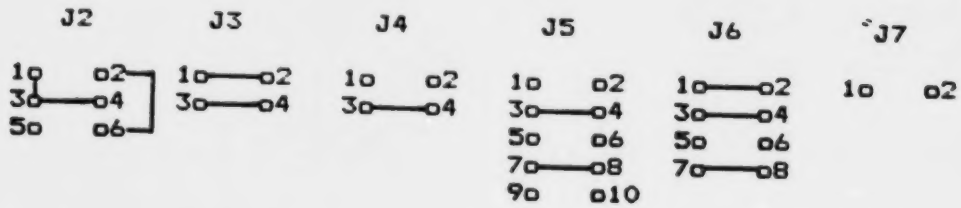
Number of input channels: 16 single ended
Input voltage range: +/- 2.5 V
I/O address: 3C-3D HEX



EXAMPLE #5

Configuration:

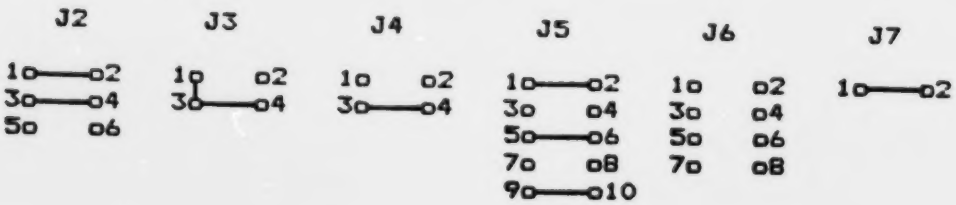
Number of input channels: 16 single ended
Input voltage range: +/- 10 V (REQUIRES +/- 15 VDC SUPPLIES)
I/O address: 8-A HEX



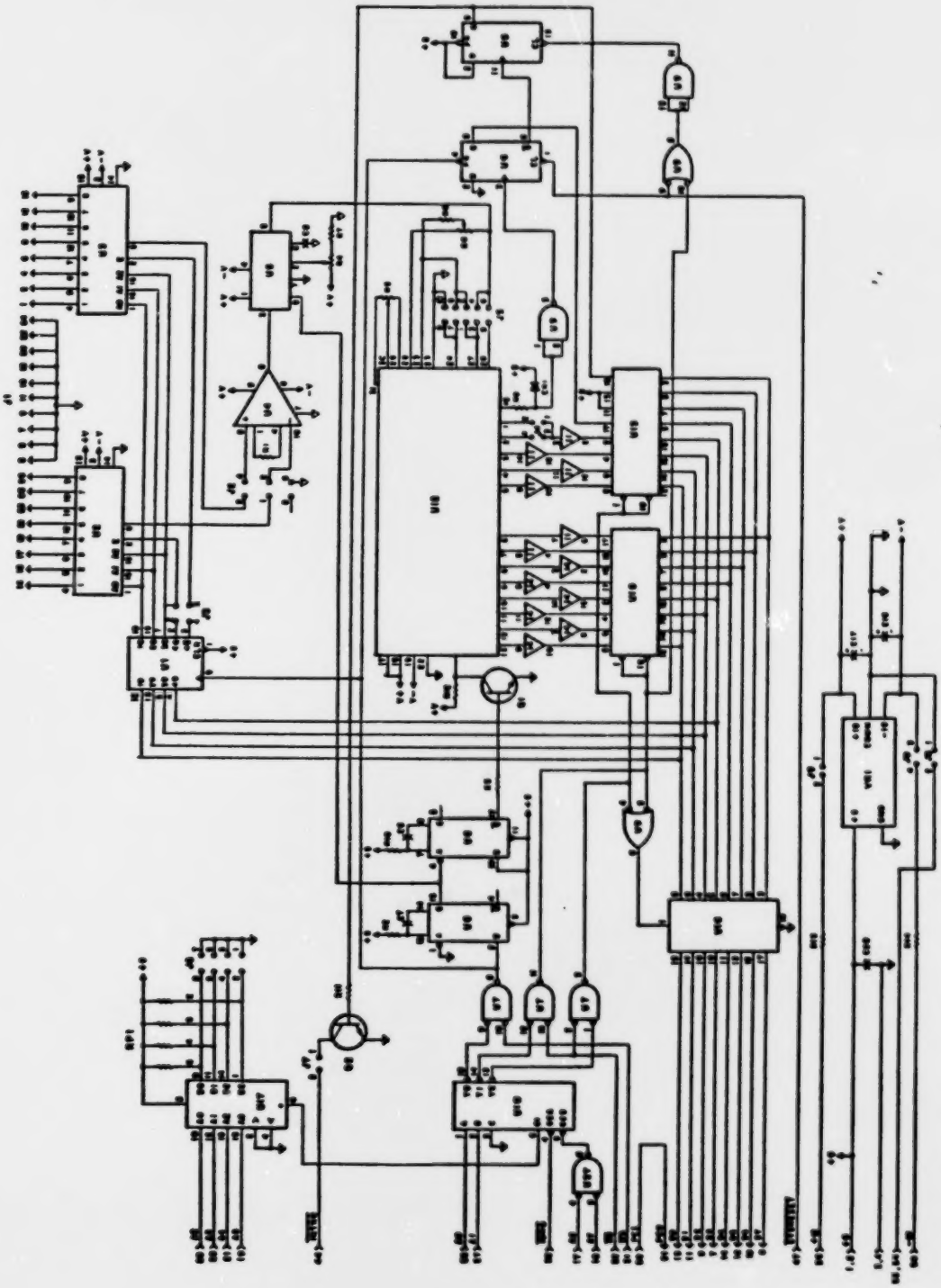
EXAMPLE #6

Configuration:

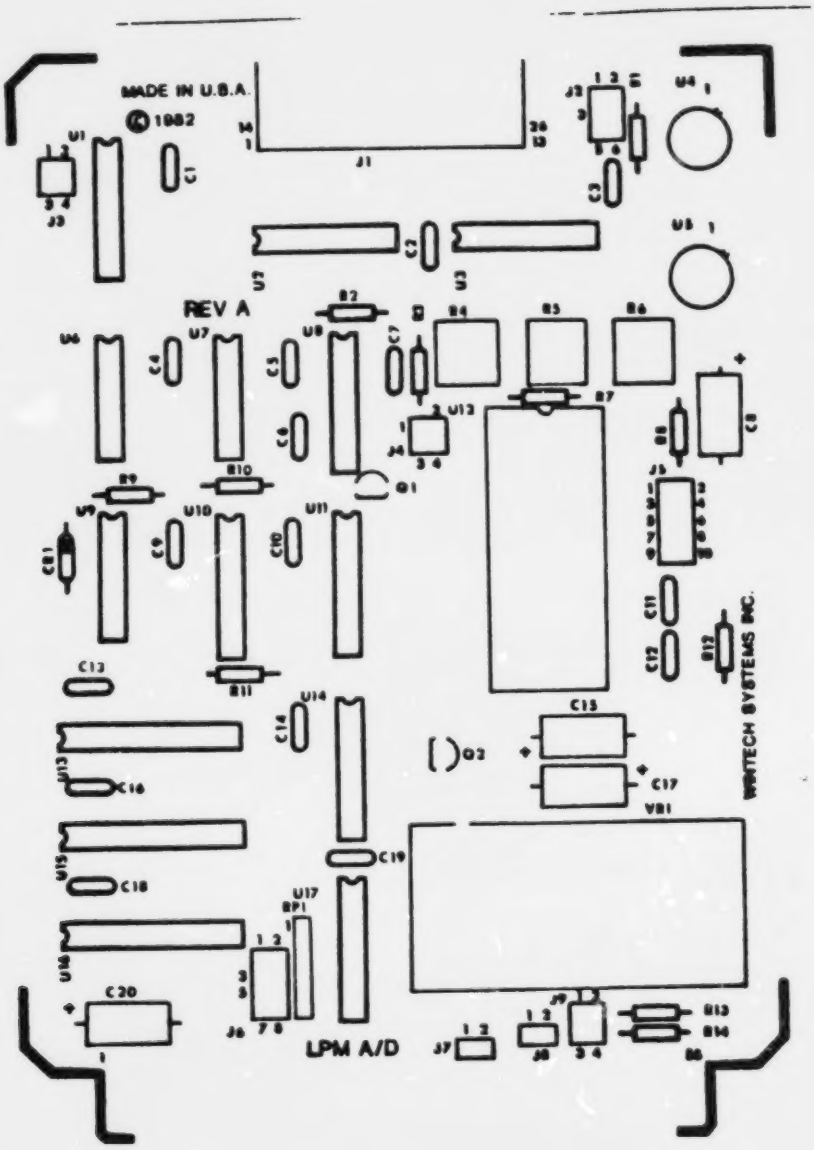
Number of input channels: 8 differential
Input voltage range: 0-5V
I/O address: 3C-3E HEX
Interrupts: enabled



SCHEMATIC DIAGRAM



PARTS PLACEMENT DIAGRAM


MADE IN U.S.A.
©1982
REV A
WINTECH SYSTEMS INC.
LPM A/D
WINTECH

PARTS LIST

LPM-A/D

QUAN	DESCRIPTION	DESIGNATOR
1	TC40H175	U1
2	HI3-508A-5	U2,U3
1	INA-101AM	U4
1	SHC-298AM	U5
1	TC40H074	U6
1	TC40H032	U7
1	74C221	U8
1	TC40H000	U9
1	TC40H138	U10
2	CD4050	U11,U14
1	ADC-HC12BMR	U12
2	TC40H244	U13,U15
1	TC40H245	U16
1	74HC85	U17
	USER OPTION	R1
1	68K 5% 1/4W	R2
4	10K " "	R3,R9,R11,R12
1	1K CERMET TRIMPOT	R4
2	10K CERMET TRIMPOT	R5,R6
1	21.5K 1% 1/8W	R7
1	470 K 5% 1/4 W	R8
2	10 OHM 5% 1/4W	R13,R14
1	10K 6 PIN SIP	RP1
1	15K 5% 1/4 W	R10
13	.1 UF CERAMIC	C1-5,C9-14,C16,C18,C19
1	500 PF MICA	C6
1	1000 PF MICA	C7
1	.01 UF POLYPROP	C8
3	22UF ELECTROLYTIC	C15,C17,C20
2	2N2222	Q1,Q2
1	1N914	CR1
1	26 PIN MALE HEADER	J1
1	6 PIN TERM STRIP	J2
2	4 PIN TERM STRIP	J3,J4
1	10 PIN TERM STRIP	J5
1	8 PIN TERM STRIP	J6
1	2 PIN TERM STRIP	J7
1	CARD EJECTOR	

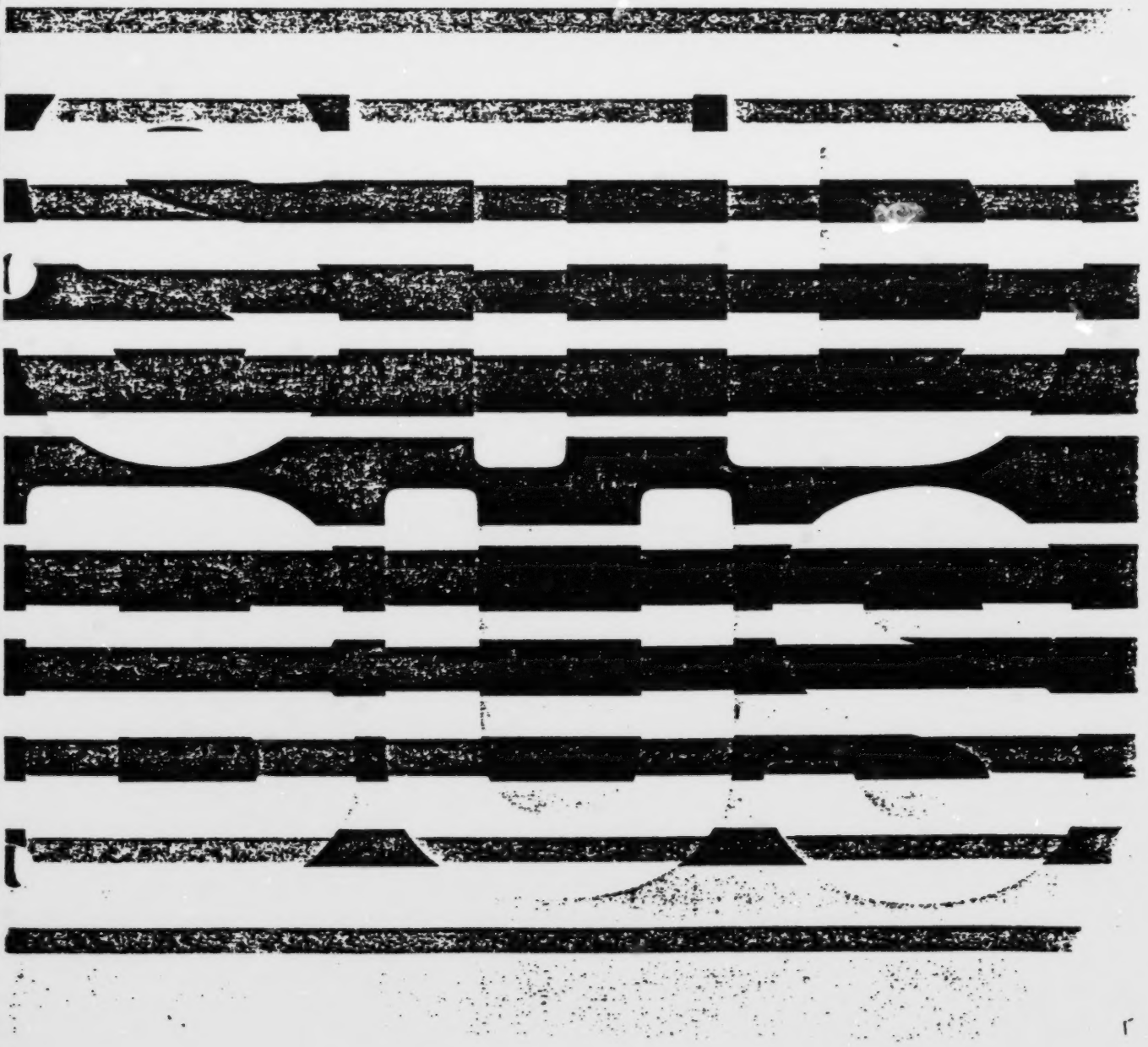
APPENDICE E
CARTE CPU (78C15)

PRO-LOG®
CORPORATION

STD 7000

78C15
80C85A Processor Card

USER'S MANUAL



FOREWORD

This manual explains how to use the Pro-Log 78C15 Processor Card. It is structured to reflect the answers to basic questions you might ask yourself about the 78C15. We welcome your suggestions on how we can improve our instructions.

The 78C15 is part of the Pro-Log Series 7000 STD BUS hardware. Our products are modular, and designed and built with second-sourced parts that are industry standards. They provide industrial managers with the means of using their own people to control the design, production, and maintenance of the products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, we teach courses on how to design with and use microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: the Microprocessor User's Guide and the Series 7000 STD BUS Technical Manual. If you would like a copy of these documents, please write to us on your company letterhead.

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Series 7000 STD BUS Technical Manual, Monterey, CA: Pro-Log Corporation.

HS-C^{2}MOS Integrated Circuits Technical Data, 2nd edition, Tokyo,Japan: Toshiba Corporation, 1983 K 4107.

1983 Microprocessor and Peripheral Handbook, Santa Clara, CA: Intel Corporation, 210844: pps 2-10 through 2-25.

1979 MCS-80/85 Family User's Manual, Santa Clara, CA: Intel Corporation, 121506-001.

High Speed CMOS Logic Data, Austin, TX: Motorola Inc., DL129.

Section 1

PURPOSE AND MAIN FEATURES

Purpose

The 78C15 processor card combines a buffered and fully expandable 80C85A microprocessor with four 8K-byte memory sockets. Each socket accepts CMOS RAM or EPROM parts.

An input and an output connector are provided to access the 7.5, 6.5, and 5.5 interrupt pins, the serial input data (SID) and serial output data (SOD) pins, and a programmable Segment select (SGMT) pin.

Fully implemented in high speed CMOS, the 78C15 offers high noise immunity, low power consumption, and a wide temperature range. It is designed to be used with other CMOS cards on the STD BUS.

The 78C15 responds to the STD BUS signal BUSRQ* allowing direct memory access (DMA) to other cards in the system.

FEATURES

- High speed CMOS: High noise immunity, low power consumption, wide temperature range
- CMOS 80C85A processor
- 32K-byte capacity, four 8K by 8 RAM/EPROM memory sockets
- DMA to onboard memory sockets
- 4.0 MHz crystal
- User connections for 80C85A interrupts, SID, and SOD
- Advanced power-on reset circuit with Vcc sensing
- MEMEX and Segment select (SGMT) memory expansion control
- Single +5V operation
- Gold-plated, precision-machined pin sockets, connectors, and jumper posts

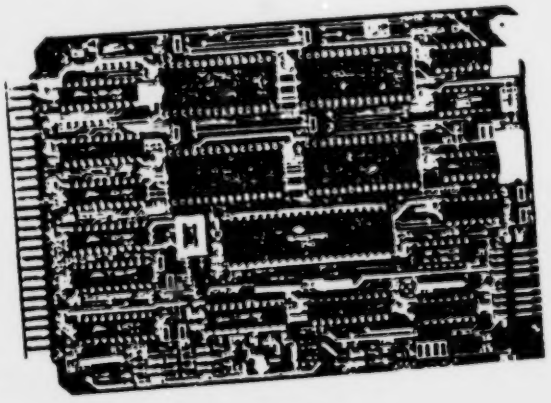


Figure 1-1. Processor Card (78C15)

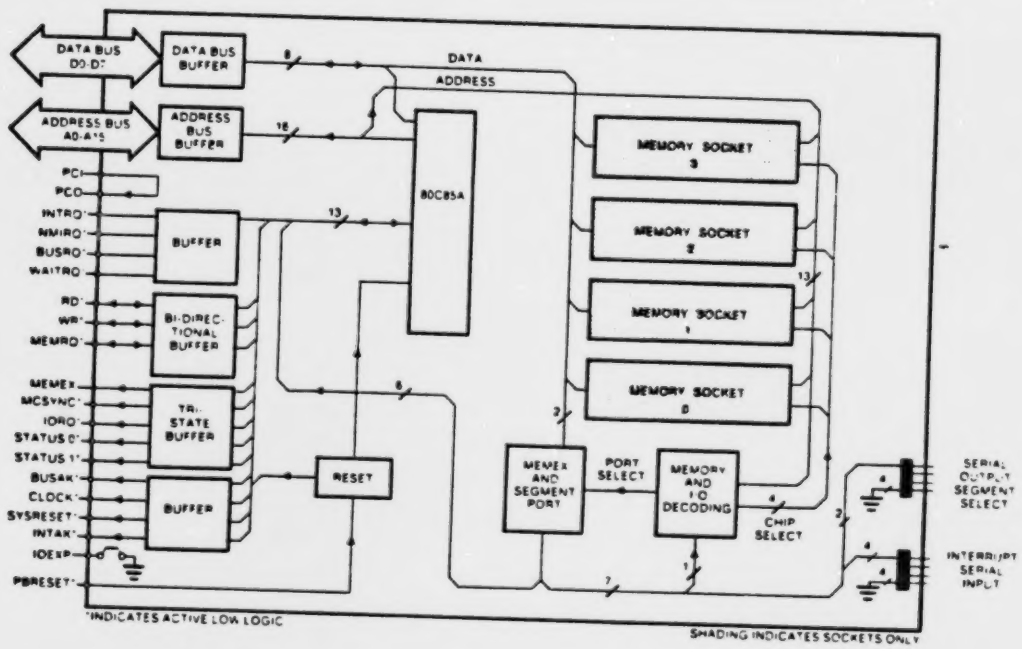


Figure 1-2. Block Diagram (78C15)

Functional Description

This portion of section 1 describes the function of each block of circuitry shown in the functional block diagram of figure 1-2.

CMOS 8085A CPU — The CMOS 8085A CPU is a CMOS version of the industry standard 8085A. All the functions, features, and capabilities of an 8085A are coupled with the advantages of CMOS technology; high noise immunity, low power consumption, and wide temperature range. The result is a CPU with proven features that can use existing software and that can be used under extreme conditions.

ONBOARD MEMORY — The onboard memory consists of four 28-pin sockets. This memory can be up to 32K bytes consisting of any combination of four 8K by 8 RAMs or ROMs.

MEMORY DECODE — The memory decode consists of an 8K by 8 memory decoder. This circuitry decodes the memory address lines into 8K blocks to select the addressed memory socket. For more information, see section 2, Installation and Specifications.

I/O DECODE — The I/O decode section selects the onboard port and decodes the address lines only during an I/O write cycle. MEMEX and Segment can be written through the onboard port.

RESET — The reset circuit resets the CPU during power-up or during a pushbutton reset. During power-up, the circuit keeps the CPU in a reset state until the power supply reaches a voltage in the proper operating range. This delay ensures that the CPU has a valid power supply when it leaves reset, which prevents latch-up. The pushbutton reset circuit debounces the pushbutton input.

MEMEX AND SEGMENT PORT — Both the STD BUS memory expansion line, MEMEX, and the user card edge memory expansion line, Segment, are controlled by the on-card port of the 78C15. Both signals provide control to expand memory for large systems. See section 3, Operation and Programming, for more detail.

Section 2

INSTALLATION AND SPECIFICATIONS

Introduction

This section covers all aspects of the 78C15 which need review before operating it, including optional functions selected by jumpers, cables used, and installation. Complete specifications for the 78C15 are included at the end of this section.

Installation

The 78C15 can operate by itself or as part of an STD BUS system. The card should be installed in an STD BUS backplane or card rack with the card ejector toward the top, as shown in figure 2-1. The card can be installed into any slot in the rack.

CAUTION

TO PREVENT POSSIBLE DAMAGE TO YOUR STD BUS SYSTEM, MAKE SURE THAT POWER IS **OFF** BEFORE INSERTING A CARD INTO THE RACK OR BEFORE REMOVING A CARD FROM THE RACK.

If access to the card is needed for testing or servicing, a card extender may be used, such as the Pro-Log 7901.

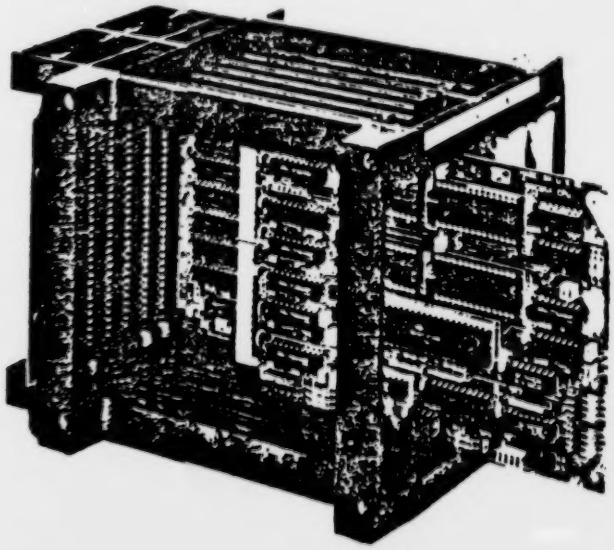


Figure 2-1. Installation in STD BUS Card Rack
(For reference only)

CMOS Precautions

1. An input to a CMOS gate should not exceed its power supply range. If a high level input exceeds the power supply voltage, current will flow into the input through the input protection diode. This may result in latch-up or damage.

2. Because of this restriction, in systems using two power supplies special attention should be paid to: the relative voltage level of the two supplies when each supply is turned on and the difference in rise and fall times between the two supplies. One way to avoid possible problems when using two supplies is to connect them to each other directly or through diodes.

3. To prevent damage to CMOS components by static discharge, the card should always be stored in a conductive carrier. Individuals and tools should be grounded before coming in contact with the card.

Termination and Loading

A termination network is not required for Pro-Log CMOS STD BUS systems. (In fact, using the Pro-Log 7909A terminator card in a CMOS STD system will degrade the system performance as a result of its capacitive loading.)

Since the input impedance of CMOS is very large, the main restriction on fanout is load capacitance. As the total capacitive load on an output is increased, the propagation delays increase along with power consumption. Since the Pro-Log 24-slot 7106 motherboard uses termination that presents a large capacitive load, it should not be used with CMOS cards. The user should check any other termination in the system for capacitive and DC loading.

Jumpers

There are several optional functions on the 78C15 which are selected by jumpers. Most of the jumpers are wirewrap posts which can be shorted by supplied shorting plugs (Elco Corporation, part number 00 8261 02 42 00 870) or by wire-wrapping. Some of the card jumpers are soldered wire. To disconnect these, cut each wire jumper in two places to prevent reshorting. The wire jumpers can be replaced with a pair of wirewrap posts (Elco Corporation, part number 00 8261 02 32 00 852). When removing wire jumpers, be sure to cut them and remove one half at a time to prevent circuit trace damage.

Cabling

The J1 Segment connector can use a Pro-Log RC704-1 or RC704-2 cable. These cables are one (RC704-1) or two (RC704-2) feet of twisted pair wires with a 2-pin connector on each end. These cables mate to the card responding to Segment (e.g., the Pro-Log 77C08 CMOS 64K-byte memory card).

Mechanical Specifications

The 78C15 meets all general mechanical specifications of the STD BUS. Refer to the STD Specification and Practice for outline dimensions.

Jumper Options

The 78C15 has several optional functions which are selected by jumpers. Figure 2-2 shows the jumper locations and figure 2-3 lists their functions. After reviewing the jumper options available, check to be certain the card is properly configured to your specific application before installing it in the system.

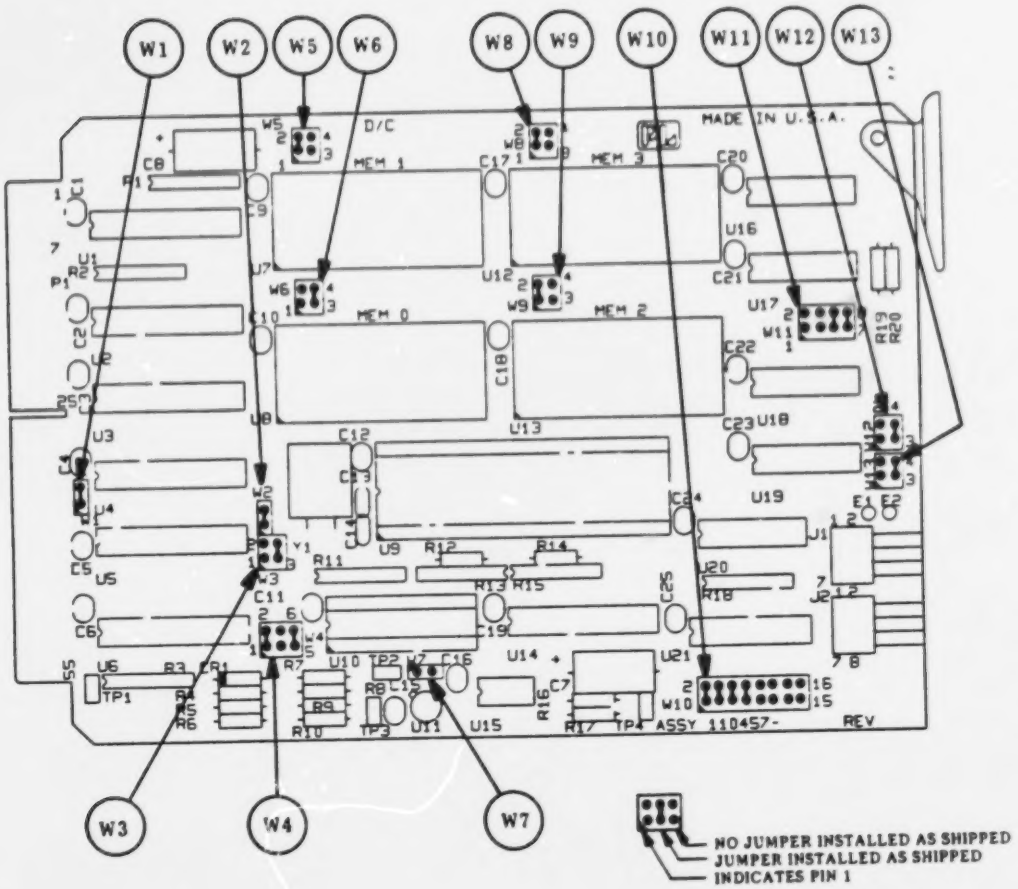


Figure 2-2. Jumper Locations (78C15)

JUMPER	PINS	DESCRIPTION	JUMPER INSTALLED AS SHIPPED
W1	1-2 no jumper	IOEXP is connected to ground. IOEXP must be controlled by another card.	1-2
W2	1-2 no jumper	The 78C15 controls MEMEX. MEMEX must be controlled by another card.	1-2
W3	1-2 3-4 no jumper	On-card memory responds to MEMEX high if enabled. On-card memory responds to MEMEX low if enabled. On-card memory is independent of MEMEX.	3-4
W4	1-2 3-4 5-6	Connects the J2-8 RS5.5* pin to the RST5.5 8085 input. Connects the STD INTRQ* signal to the RST5.5 8085 input. Connects the STD INTRQ* signal to the 8085 INTR (interrupt) input.	1-2,5-6
W6, W5, W9, W8	1-2 3-4	Configures the memory socket (MEM 0 - MEM 3 respectively) for a 28-pin 8K x 8 RAM device. Configures the memory socket for 28-pin 8K x 8 ROM or EPROM.	3-4 MEM 0 1-2 MEM 1 1-2 MEM 2 1-2 MEM 3
W7	no jumper	For Pro-Log use only	no jumper
W10	no jumper 1-2 thru 7-8 9-10 thru 15-16	Disables all onboard memory. Enables memory sockets (MEM 0-3 respectively) in the lower 32K address range (0000_H-$7FFF_H$). Enables memory sockets (MEM0-3 respectively) in the upper 32K address range (8000_H-$FFFF_H$).	1-2 thru 7-8
W11	1-2, 3-4 5-6,7-8 no jumper	MEMEX and Segment control port address is 7F. MEMEX and Segment control port address is FE. Control port is disabled	5-6,7-8
W12	1-2 3-4	Segment is low at power-up and its port is noninverting. Segment is high at power-up and its port is inverting.	3-4
W13	1-2 3-4	MEMEX is high at power-up, and its port is inverting. MEMEX is low at power-up, and its port is noninverting.	3-4

Figure 2-3. Jumper Functions (78C15)

Memory Mapping (W5,W6,W8,W9,W10)

The 78C15 processor card contains four 28-pin sockets for 8K by 8 CMOS bytewide memories. Using the W10 jumpers, the 78C15 memory sockets can be mapped to either the upper or lower 32K address space and may be enabled (jumper in) or disabled (jumper out) on 8K boundaries. The card may be mapped as shown with the W10 jumpers. Unused sockets on the card can be disabled for off-card use by removing the appropriate W10 jumper.

		W10			
CHIP REF.	MEMORY SOCKET	UPPER ADDRESS	LOWER ADDRESS		TYPE
U8	MEM 0 0000-1FFF	pins 1-2 8000-9FFF	pins 9-10	W6	1-2 RAM 3-4 EPROM (as shipped)
U7	MEM 1 2000-3FFF	pins 3-4 A000-BFFF	pins 11-12	W5	1-2 RAM (as shipped) 3-4 EPROM
U13	MEM 2 4000-5FFF	pins 5-6 C000-DFFF	pins 13-14	W9	1-2 RAM (as shipped) 3-4 EPROM
U12	MEM 3 6000-7FFF	pins 7-8 E000-FFFF	pins 15-16	W8	1-2 RAM (as shipped) 3-4 EPROM

Figure 2-4. Memory Mapping and Type

Memory Devices

The 78C15 processor card uses CMOS bytewide memory components which are compatible with the 28-pin JEDEC standard. To use other memory components, compare the manufacturers' data sheets to the socket configurations, check for any special requirements, and be sure they are designed to be used with CMOS logic. Figure 2-5 shows components which are compatible on the 78C15 card.

MANUFACTURER	CHIP	ACCESS
Fujitsu MBM 27C64	8K x 8 CMOS EPROM	300 ns
Hitachi HM 6264P	8K x 8 CMOS SRAM	150 ns

Figure 2-5. Compatible Memory Devices (78C15)

Memex and Segment (W2,W3,W12,W13)

MEMEX and Segment are both controls for expanded memory schemes. For more detailed information, see section 3, Operation and Programming.

Several jumpers affect MEMEX. W3 determines how MEMEX affects onboard memory. Figure 2-6 shows the position of W3 in relationship to MEMEX.

W3 JUMPER POSITION	ONBOARD MEMORY ENABLED WHEN
1-2	MEMEX high
3-4*	MEMEX low

* As shipped configuration

Figure 2-6. MEMEX Affecting Onboard Memory

If no pins of W3 are jumpered, the onboard memory is permanently enabled regardless of the state of MEMEX. Jumper W13 determines the state of MEMEX after reset (when controlled by the 78C15) and whether the data written to the MEMEX port is to be inverted. Figure 2-7 shows the possible configurations.

W13 PIN NUMBER	STATE AFTER RESET	DATA FROM PORT
1-2	MEMEX high	inverted
3-4*	MEMEX low	noninverted

* As shipped configuration

Figure 2-7. MEMEX Port Configuration

Jumper W2 determines which card controls MEMEX. With the jumper installed MEMEX is controlled by the 78C15. Otherwise MEMEX is left floating to be controlled by another card. W12 determines the state of Segment after reset and whether the data written to the Segment port is to be inverted. Figure 2-8 shows the possible configurations.

W12 PIN NUMBER	STATE AFTER RESET	DATA FROM PORT
1-2	Segment low	noninverted
3-4*	Segment high	inverted

* As shipped condition

Figure 2-8. Segment Port Configuration

Onboard Port (W11)

Jumper W11 affects the configuration of the onboard port through which data for MEMEX and Segment are passed. Jumper W11 determines the address of the port. Figure 2-9 shows the possible configurations.

W11 PIN NUMBERS	PORT ADDRESS
1-2, 3-4	Port 7F
5-6, 7-8*	Port FE
No Jumpers	Port Disabled

* As shipped configuration

Figure 2-9. Onboard Port Configuration

Interrupt Jumper (W4)

Jumper W4 provides the user flexibility when using the 80C85A interrupts. Pins 1 and 2 connect the RS5.5* signal (user edge connector J2 - pin 8) to the 80C85A RST5.5 input (pin 9). Jumper positions 3-4 and 5-6 determine the type of processor interrupt caused by the STD BUS INTRQ* signal. Jumper 3-4 connects INTRQ* to the 80C85A RST5.5 input so the interrupt address is $002C_H$. Jumper 5-6 connects INTRQ* to the 80C85A INTR input (pin 10) so the interrupt routine address must be available to the CPU on the data lines during interrupt acknowledge. When using this option, an interrupt controller card which supplies an interrupt address vector should be used. As an alternative, the STD data lines may be pulled up with resistor networks R1 and R2 which provide an FF interrupt vector address to the 80C85A. The designer must determine the value of the pullups which satisfies the timing and loading tradeoffs of each CMOS system.

NOTE: To prevent erroneous interrupts, W4 should be configured to either pins 1-2 and 5-6 or 3-4 only.

User Connectors

The J1 and J2 connectors allow the user to access several pins on the 80C85A chip in addition to a general output line (SGMT). The J1 connector pins are outputs only: The J2 pins are inputs only. Each signal pin is paired with a ground pin for use with twisted pair interconnect cables such as the Pro-Log RC704-1 and RC704-2 cables.

The J1 connector contains a digital output line (SGMT, pin 6), a serial output data line (SOD, pin 8), and two spare lines with PCB pads (pins 2 and 4). The J2 connector contains the serial input data line (SID*, pin 2) and the 80C85A vectored interrupt lines: RS7.5*, RS6.5*,and RS5.5* (pins 4,6, and 8 respectively).

J1 (OUTPUT) and J2 (INPUT) PIN LOADING

	MNEMONIC	INPUT (CMOS LOADS)#	OUTPUT (CMOS LOADS)#	PIN NUMBER		PIN NUMBER	OUTPUT (CMOS LOADS)	INPUT (CMOS LOADS)	MNEMONIC
J1	Spare			2	1		OUT		Ground
	Spare			4	3		OUT		Ground
	SGMT		20	6	5		OUT		Ground
	SOD*		20	8	7		OUT		Ground
J2	SID*	(1)		2	1			IN	Ground
	RS7.5*	(1)		4	3			IN	Ground
	RS6.5*	(1)		6	5			IN	Ground
	RS5.5*	(1)		8	7			IN	Ground

CMOS load = 10 pF at ±5 uA
* designates active low level logic
(1) designates load = 10 pF at 0.5 mA

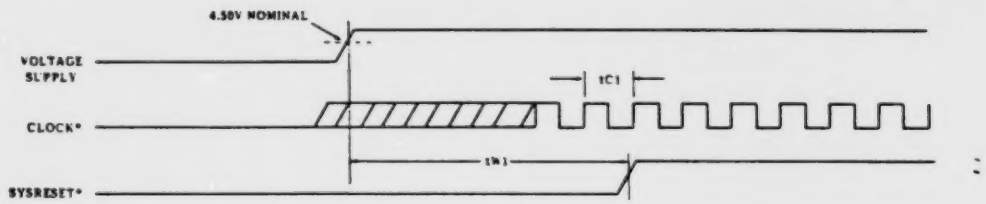
Figure 2-10. Load Characteristics & Pinouts for J1 & J2 Connectors

IOEXP (W1)

IOEXP is one of the STD BUS standard signals. IOEXP enables or expands I/O port addressing. Jumper W1 determines which card controls the IOEXP line. With the jumper installed, IOEXP is grounded by the 78C15. With no jumper, IOEXP is left floating to be controlled by another card.

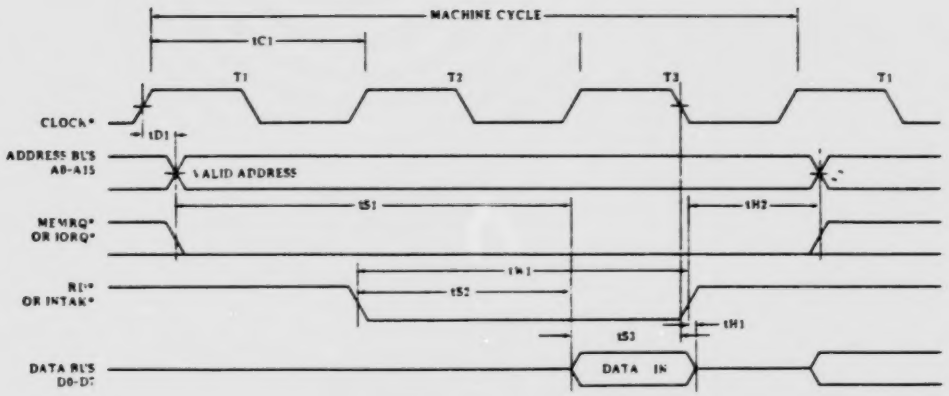
Timing Specifications

Figures 2-11 through 2-15 show the signal sequences and timing for various 78C15 functions. They show the signals as they appear at the card edge connector of the 78C15.



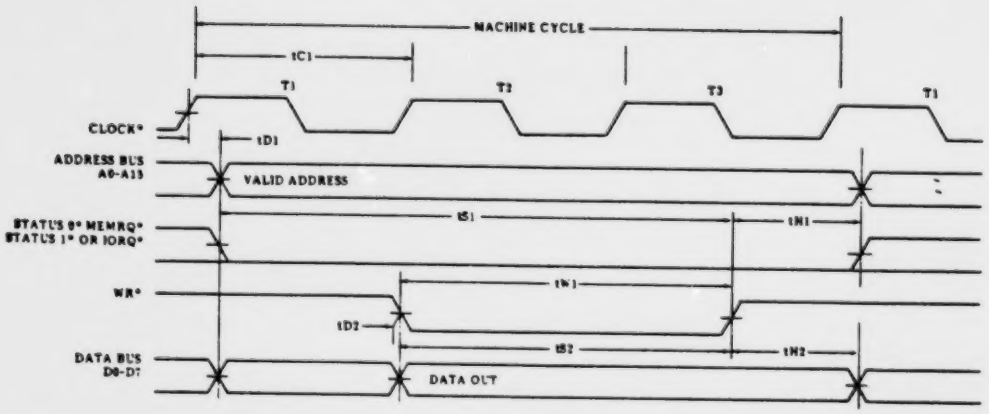
SYMBOL	PARAMETER	UNIT	4.00 MHz	
			MIN	MAX
tC1	Clock cycle time	ns		500
tW1	Power-up reset width after supply threshold	ms	25	85

Figure 2-11. Reset After Power-Up (78C15)



SYMBOL	PARAMETER	UNIT	4.00 MHz	
			MIN	MAX
tC1	Clock cycle time	ns		500
tD1	Address delay from T1 clock	ns		265
tH1	Data hold time	ns	0	
tH2	Hold time after RD*	ns	110	
tS1	Address setup before data valid	ns		950
tS2	RD* setup before data valid	ns		520
tS3	Data setup time	ns	130	
tW1	RD* pulse width	ns	570	

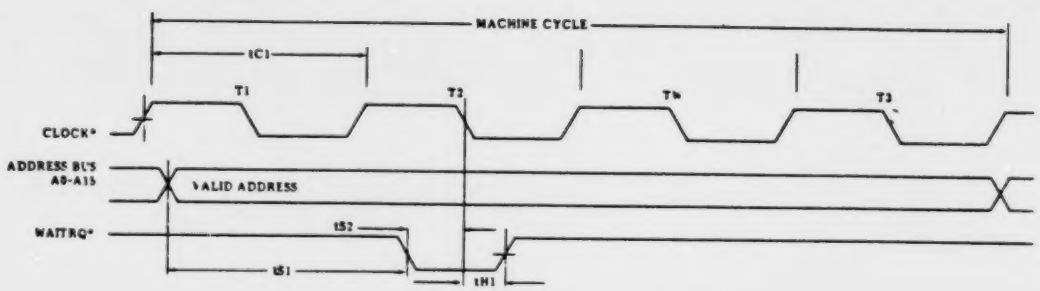
Figure 2-12. Read Timing: Memory Read, Input and Interrupt (78C15)



SYMBOL	PARAMETER	4.00 MHz MIN	4.00 MHz MAX
tC1	Clock cycle time		500
tD1	Address delay from T1 clock		265
tD2	Data delay from WR*		140
tH1	Address hold time	110	
tH2	Data hold time	85	
tS1	Address setup before write strobe	950	
tS2	Data setup time before write strobe	590	
tW1	WR* pulse width	570	

All times given in nanoseconds.

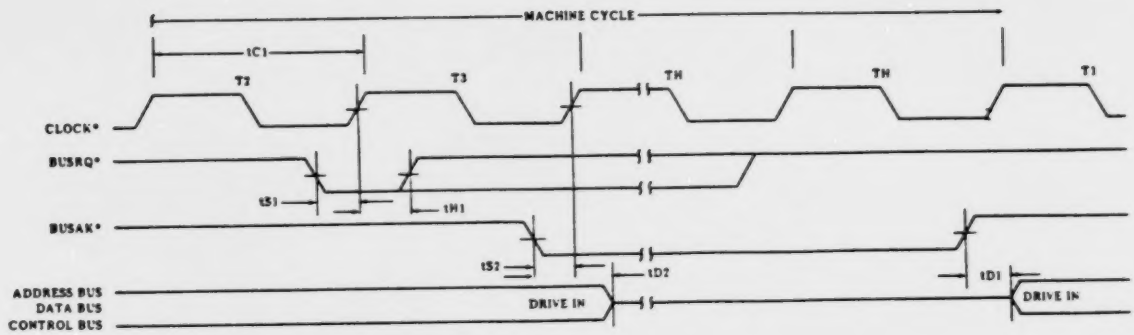
Figure 2-13. Write Timing: Memory Write and Output (78C15)



SYMBOL	PARAMETER	4.00 MHz	
		MIN	MAX
tC1	Clock cycle time		500
tH1	WAITRQ* hold time after T2/TW	0	
tS1	Address setup before WAITRQ*		450
tS2	WAITRQ* setup before T2/TW	155	

All times given in nanoseconds.

Figure 2-14. Wait Request Timing (78C15)



SYMBOL	PARAMETER	4.00 MHz MIN	4.00 MHz MAX
tC1	Clock cycle time		500
tD1	Bus delay after BUSAK* high		400
tD2	Bus delay after BUSAK* low		60
tH1	BUSRQ* hold after start of T3	0	
tS1	BUSRQ* setup prior to T3	220	
tS2	BUSAK* setup prior to TH	140	

All times given in nanoseconds.

Figure 2-15. BUS Request Timing (78C15)

Electrical and Environmental Specifications

Figures 2-16 and 2-17 show the electrical specifications for the 78C15. Environmental specifications are shown in figure 2-18. Figure 2-19 gives pinout and loading characteristics of the connection between the 78C15 and the STD BUS.

			RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS	
MNEM.	PARAMETER	UNIT	MIN	TYP	MAX	MIN	MAX
VCC	Logic Supply	V	4.50	5.00	5.50	0	7.00

Figure 2-16. Electrical Specifications (78C15)

			RECOMMENDED OPERATING LIMITS		
MNEM.	PARAMETER	UNIT	MIN	TYP	MAX
ICC*	VCC Supply Current	mA	—	15	36

Figure 2-17. Electrical Characteristics Over Operating Range (78C15)

*ICC specification assumes memory sockets are empty (as shipped). For maximum memory currents add 110 mA (max) selected, 3 mA (max) standby per 8K by 8 static CMOS RAM (Hitachi HM6264P type), and 30 mA selected, 1 mA standby per 8K by 8 EPROM (Fujitsu MBM27C64 type).

			RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS	
MNEM.	PARAMETER	UNIT	MIN	TYP	MAX	MIN	MAX
— —	Free Air Temp. Humidity	°C %RH	-40 5	+25 —	+85 95[1]	-40 5	+100°C 95[1]

[1]Noncondensing relative humidity

Figure 2-18. Environmental Specifications (78C15)

Power-on and Pushbutton Reset

Power-on reset holds the SYSRESET* line low and releases it 85 ms (max) after the VCC reaches 4.5V. The PBRESET* is debounced approximately 20 ms, and produces a 65 ms (max) SYSRESET* pulse.

Bus Interface

The 78C15 is a CMOS card designed for usé with other CMOS cards on the STD BUS using CMOS logic levels and drive characteristics. While it can be interfaced to cards using TTL logic, Pro-Log does not warrant that use.

PIN NUMBER				PIN NUMBER			
OUTPUT (CMOS LOADS)						OUTPUT (CMOS LOADS)	
INPUT (CMOS LOADS)						INPUT (CMOS LOADS)[A]	
MNEMONIC							MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	20	8	7	20	1	D3
D6	1	20	10	9	20	1	D2
D5	1	20	12	11	20	1	D1
D4	1	20	14	13	20	1	D0
A15	1	20	16	15	20	1	A7
A14	1	20	18	17	20	1	A6
A13	1	20	20	19	20	1	A5
A12	1	20	22	21	20	1	A4
A11	1	20	24	23	20	1	A3
A10	1	20	26	25	20	1	A2
A9	1	20	28	27	20	1	A1
A8	1	20	30	29	20	1	A0
RD*	1	20	32	31	20	1	WR*
MEMRQ*	1	20	34	33	20		IORQ*
MEMEX	[2]	20	36	35	OUT		IOEXP
MCSYNC* (ALE*)		20	38	37			REFRESH*
STATUS 0* (S0*)		20	40	39	20		STATUS 1* (S1*)
BUSRQ* (HOLD*)	[1]		42	41	20		BUSAK* (HLDA*)
INTRQ* (INTR*)	[1]		44	43	20		INTAK* (INTA*)
NMIRQ* (TRAP*)	[1]		46	45		[1]	WAITRQ* (READY)
PBRESET* (R*)	B		48	47	20		SYSRESET* (RST*)
CNTRL*(EXT CLK IN)			50	49	20		CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

A CMOS load = 10 pF at ±5 uA
B Switch Input
* Designates active low-level logic
() Designates equivalent 80C85A pin names
1 Designates load = 10 pF at 0.5 mA
2 Designates load = 20 pF at 0.5 mA

Figure 2-19. STD BUS Edge Connector Pin List (78C15)

Section 3

OPERATION AND PROGRAMMING

Introduction

This section describes the theory of operation for the 78C15. The following describes the operation of the power-on/pushbutton reset circuit and memory expansion (MEMEX and Segment) control. All references are made to the schematic in section 5.

Power-on and Pushbutton Reset Circuit

The 78C15 reset circuit consists mainly of two voltage comparators. The first comparator will not turn on until the power supply reaches a voltage in the operating range. After the first comparator turns on, indicating a valid operating voltage, RESET* must be held low until the clock oscillator is functioning. This is accomplished by having the first comparator charge an RC network, which forms an input to the second voltage comparator. The second comparator will turn on and set RESET* high after an RC time constant equal to the oscillator start up time (85 ms maximum).

R9 and U11 generate a reference voltage for the two comparators. R5 and R6 form a voltage divider for the supply voltage. R3-6 (10K) and C7 form the oscillator startup RC time constant network. R8 and R17 provide hysteresis for the voltage comparators to prevent oscillations.

The remainder of the reset circuit is associated with a pushbutton reset. The pushbutton input is debounced by a circuit consisting of a comparator (U15) and an RC network (R7 and C7). The PBRESET* is effectively wire-ORed with the power-on reset signal through CR1 and becomes the RESET* signal.

Memex and Segment Control

Both MEMEX and Segment allow the capacity of the system memory to be expanded. MEMEX is implemented through the STD BUS, where Segment is implemented through the user connector J1. Since MEMEX is on the STD BUS, it is a signal that can be used by any card. Segment, on the other hand, is only used when it is connected by cable to a card that responds to Segment. Other than this difference, MEMEX and Segment are the same. In the following theory description MEMEX is used, but the theory holds true for Segment as well.

MEMEX allows the user to select between two banks of memory. To use MEMEX, the program writes to the on-card port. MEMEX uses bit D0 of the port, and Segment uses bit D1. Writing to the port immediately affects the memory expansion line polarities. MEMEX affects the entire system, since it is an STD BUS signal. Segment affects only the card to which it is connected.

Figure 3-1 shows a system with 96K of memory. The on-card memory consists of four 8K by 8 ROMs residing at addresses 0000-7FFF. This memory is permanently enabled and can be addressed whether MEMEX is high or low. The other 64K block is RAM and is divided into two 32K banks on separate cards. Both banks reside at addresses 8000-FFFF. One bank is enabled by MEMEX low and the other is enabled by MEMEX high. With this scheme, the main part of the software driver can reside in the on-card memory at addresses 0000-7FFF. This main program will use MEMEX to switch back and forth between the two banks of RAM.

Figure 3-2 shows a system with 128K of memory split into two 64K banks. Both banks reside at addresses 0000-FFFF. The on-card memory sockets of the 78C15 are not used, and are disabled by removing the associated jumpers (see section 2, Installation and Specifications). Therefore, MEMEX does not affect the on-card memory at all. The software drivers for this system must be located in both banks of memory, because once control is switched to the other bank there is no way to get back without the driver. For example, if the system driver program in the primary bank changed MEMEX high and there were no driver in the secondary bank, there would be no instructions to send MEMEX low and send the processor back to the primary bank. There must be some kind of memory bank control in both banks.

When switching MEMEX, the address of the present memory location does not change. For example, in the system shown in figure 3-2, if the program counter that holds the address of the next instruction were pointing at 4000 in the primary memory bank and MEMEX were switched high, the program counter would still be pointing to 4000, but in the secondary memory bank. Once at that point any instruction may be executed, but it must be located at address 4000. To use MEMEX you must know where you are in memory in both banks so control is not lost switching between banks.

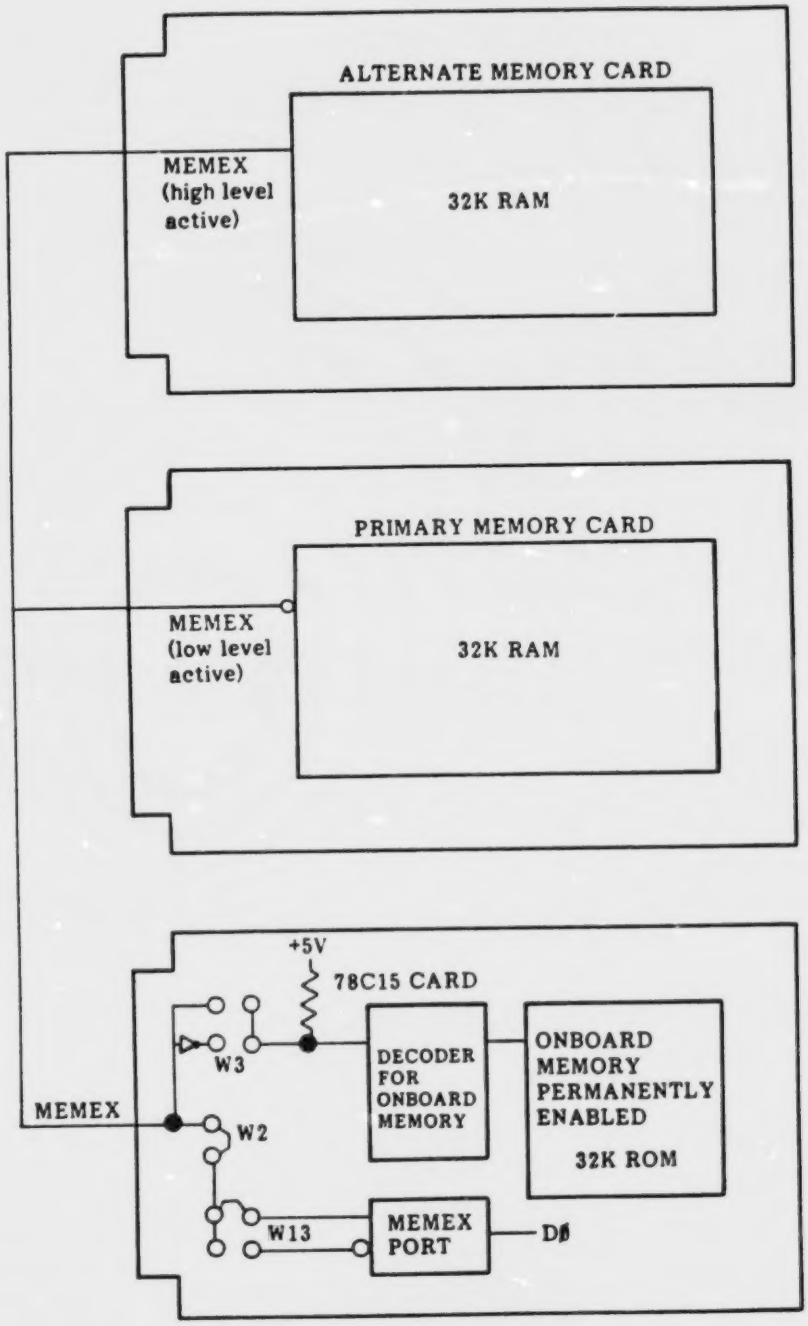


Figure 3-1. Example of MEMEX for Selecting Between Two Banks of Memory in a 96K Memory System.

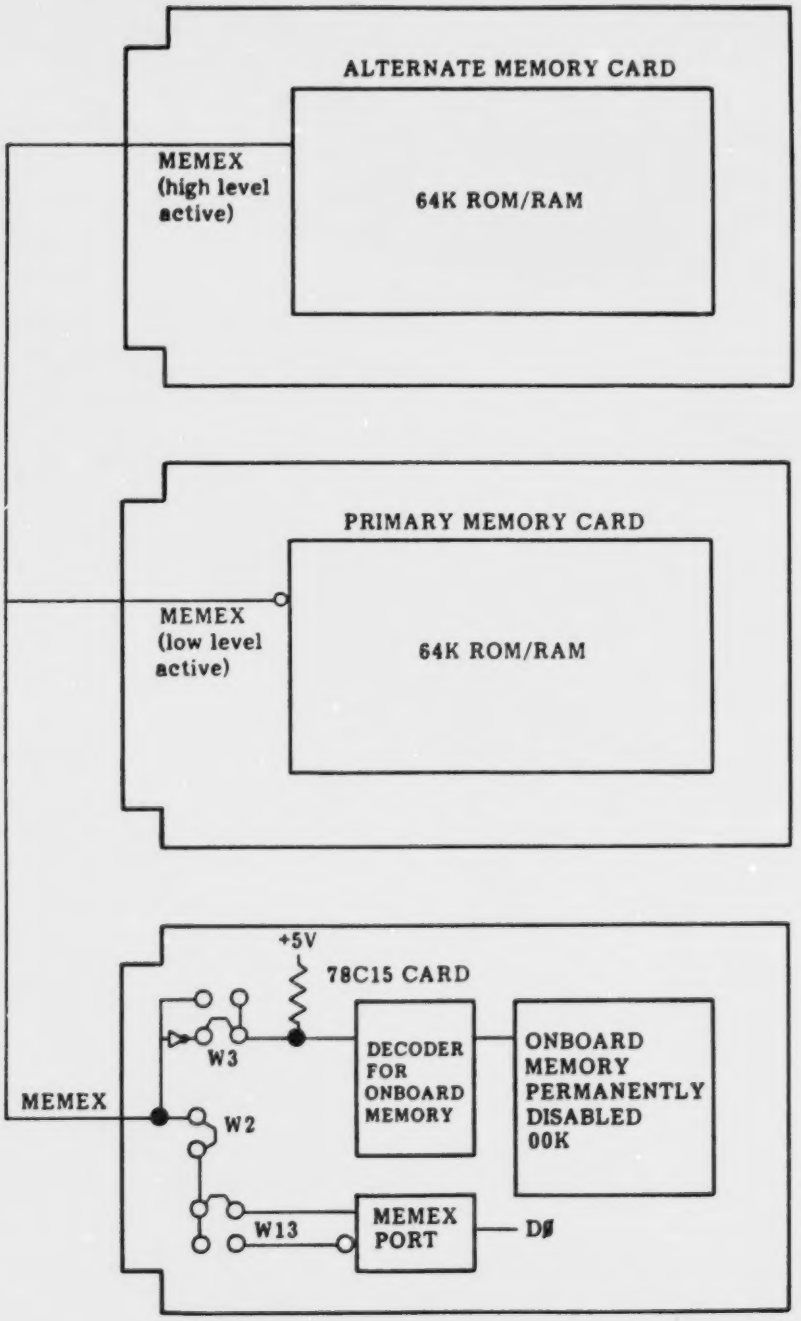


Figure 3-2. Example of MEMEX for Selecting Between Two Banks of Memory in a 128K System

Section 4

OPERATING SOFTWARE

Section 4 normally contains software subroutines to aid in using Pro-Log Series 7000 STD BUS cards. The 78C15 card requires no special operating software.

Reference Drawings

The schematic (figures 5-1 and 5-2) and assembly drawing (figure 5-3) in the following pages are included in this manual FOR REFERENCE USE ONLY. Because improvements may have been made after this manual was published, they may differ in some respects from the card and documentation that the user received from Pro-Log.

The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.

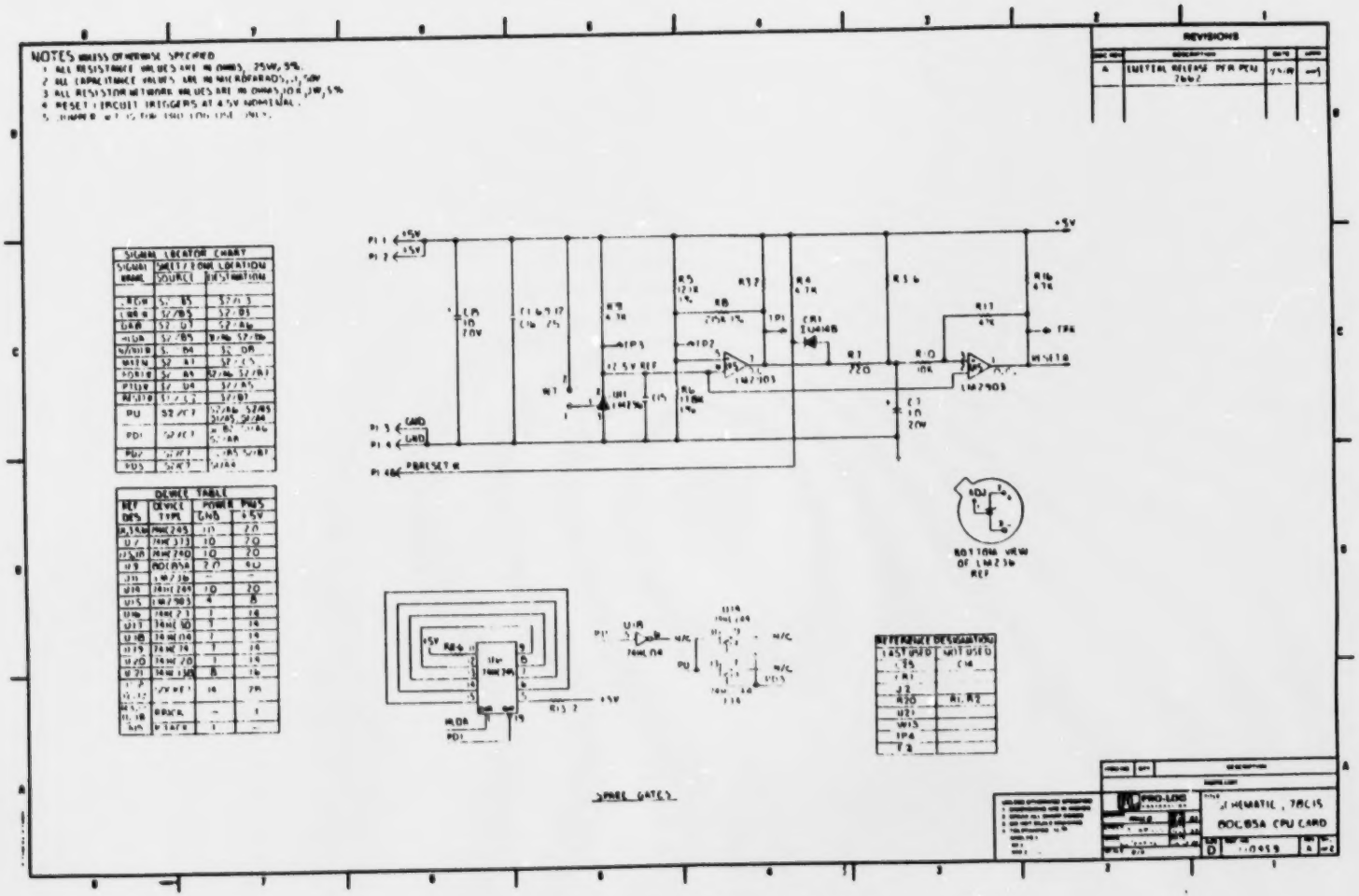


Figure 5-1. Schematic (sheet 1) for 78C15 (Reference Only)
(Refer to the documents shipped with the card)

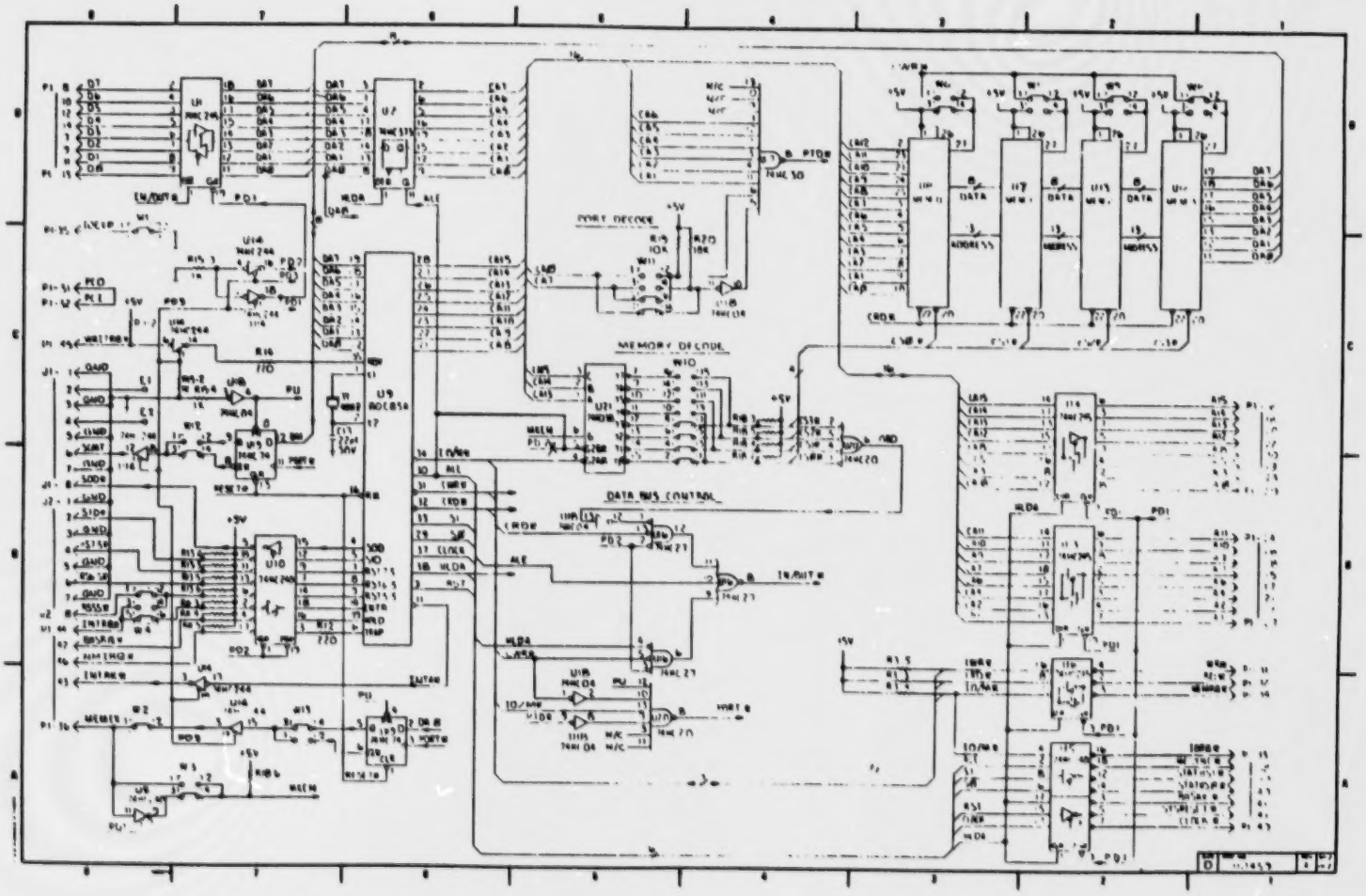


Figure 5-2. Schematic (Sheet 2) for 78C15 (Reference Only)
(Refer to the documents shipped with the card)

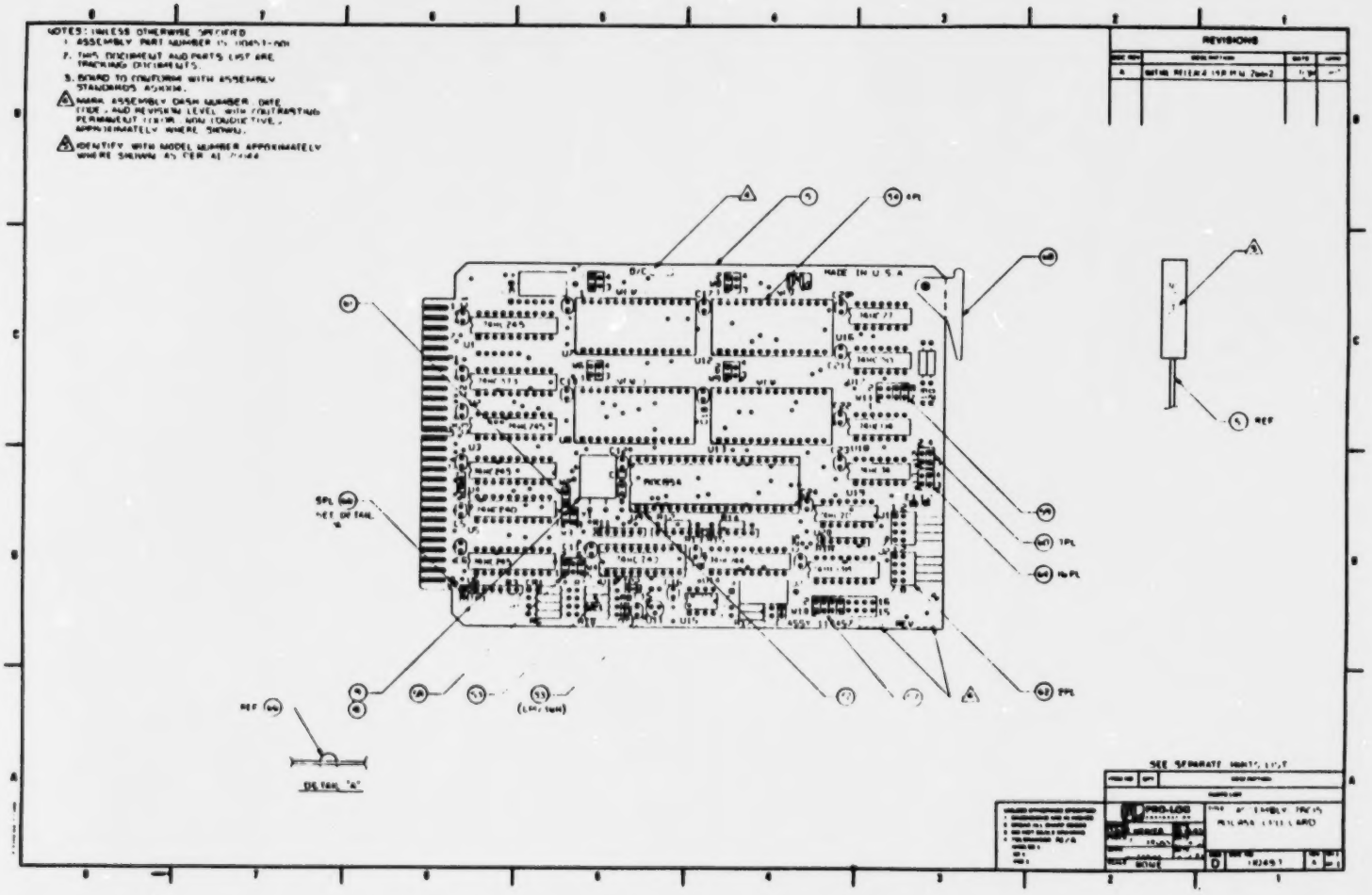


Figure 5-3. Assembly for 78C15 (Reference Only)
(Refer to the documents shipped with the card)

APPENDICE F
CARTE CALENDRIER/HORLOGE
(MCM - CLK)

CRIQ

WINTECH SYSTEMS
A STD BUS COMPANY
P.O. BOX 191361
ARLINGTON, TX 76012
817-274-7553

OPERATIONS MANUAL

MCM-CLK

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		PARTS PLACEMENT DIAGRAM	
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SECTION 1

GENERAL INFORMATION

1.1 FEATURES

- STD BUS Calendar Clock Board
- Uses the MM58167A Calendar Clock Chip
- 24 Hour Clock with BCD format
- Power Fail Detect Circuit
- On-Board Lithium Battery for Power Down Operation
- Single +5 volt supply
- STD BUS Compatible
- One Year Warranty

1.2 GENERAL DESCRIPTION

1.2.1 The MCM-CLK from Wintech Systems is a state-of-the-art, STD BUS compatible, calendar clock board that uses the National Semiconductor MM58167A calendar clock chip. The MCM-CLK provides ten thousandths of seconds, hundredths and tenths of seconds, seconds, minutes, hours, day of week, day of month, and month. In addition, the MCM-CLK also provides 56 bits of RAM for power down storage. The data from the MCM-CLK is BCD, 24 hour format. A power detect circuit and a long life Lithium battery is included to allow the calendar clock to operate in a low power mode when the system power is removed.

1.3 SPECIFICATIONS

WORD SIZE
Data 8 bits

SYSTEM CLOCK
4.0 MHz

I/O PORTS
Calendar Clock: 32 ports 40-5F HEX

INTERFACES
System - STD BUS compatible

CONNECTORS
System - 56 pin dual 0.125 inch centers

POWER REQUIREMENTS
+ 5 VDC +/- 5% at 100 mA (max)

OPERATING TEMPERATURE
0 C to +60 C

CARD DIMENSIONS
Height - 6.50 inches
Width - 4.50 inches
Thickness - 0.50 inches

SECTION 2

USER OPTIONS

2.1. I/O PORT ASSIGNMENTS

2.1.1. The MCM-CLK occupies a total of 32 I/O ports for reading and writing data to the clock. These I/O addresses and the function of each I/O port address is shown in Table 2.0.

2.2 BATTERY JUMPER

2.2.1. The MCM-CLK has an on board Lithium battery to allow the clock to operate while the board is powered down from the system. In order to preserve the maximum shelf life of the battery, the MCM-CLK is shipped with the battery jumper J2 disconnected. Before installing the board into a system, simply connect a jumper across J2.

WARNING: DO NOT LAY THE MCM-CLK BOARD ON ANY TYPE OF CONDUCTIVE MATERIAL AS THIS WILL PREMATURILY DISCHARGE THE BATTERY.

2.3 PROGRAMMING THE CLOCK

2.3.1. Before attempting to use the MCM-CLK, it is recommended that the user read the MM58167A data sheet that is included in the appendix section of the manual.

2.3.2. The MM58167A clock chip that is used on the MCM-CLK is very easy to initialize. The clock is set up for BCD data in a twenty-four hour format. To initialize the clock, all that is required is to write to the specific I/O port location, i.e. seconds, minutes, hours, etc, and the clock will accept the data without any need for stopping the clock. It should be noted that the clock cannot be stopped from counting as long as power is applied to the chip. However, both the counters and the RAM area can be reset, but the counters begin counting as soon as the reset command is completed. An example of programming the clock is given in section 2.6.

2.4 READING THE CLOCK

2.4.1. The data from the clock is read by simply executing a I/O port read from the desired I/O address as shown in Table 2.0. No syncronization is required to read the clock, however to be sure that the clock is not read during the time that the counters are "rippling", a status bit is provided so that after each read or series of reads, the status should be checked by reading I/O port address 54 Hex. A 00 Hex indicates that all data was read properly, and a 01 Hex indicates that a rippling condition

TABLE 2.0

I/O PORT ASSIGNMENTS FOR THE MCM-CLK

HEX ADDRESS	FUNCTION
40	COUNTER-- TEN THOUSANDTHS OF SECONDS
41	COUNTER-- HUNDREDTHS AND TENTHS OF SECONDS
42	COUNTER-- SECONDS
43	COUNTER-- MINUTES
44	COUNTER-- HOURS
45	COUNTER-- DAY OF WEEK
46	COUNTER-- DAY OF MONTH
47	COUNTER-- MONTH
48	RAM-- TEN THOUSANDTHS OF SECONDS
49	RAM-- HUNDREDTHS AND TENTHS OF SECONDS
4A	RAM-- SECONDS
4B	RAM-- MINUTES
4C	RAM-- HOURS
4D	RAM-- DAY OF WEEK
4E	RAM-- DAY OF MONTH
4F	RAM-- MONTHS
50	INTERRUPT STATUS REGISTER
51	INTERRUPT CONTROL REGISTER
52	COUNTERS RESET
53	RAM RESET
54	STATUS BIT
55	GO COMMAND
56	STANDBY INTERRUPT (NOT IMPLEMENTED)
57-5F	NOT USED

occurred, and the data should be read again. See examples in section 2.6.

2.5 INTERRUPTS

2.5.1. The MCM-CLK has the capability of generating an interrupt from the MM58167A clock chip on the condition of a compare with the RAM (ALARM) or programmed intervals from 1/10 of a second to 1 month.

2.5.2. The interrupts on the MCM-CLK are controlled by the write only interrupt control register located at I/O address 51 Hex, the read only interrupt status register located at I/O address 50 Hex, and the interrupt enable jumper J3.

2.5.3. To enable interrupts on the MCM-CLK, the jumper J3 must be connected. To select the type of interrupt to be generated, i.e. compare or interval, a control word must be written to the interrupt control register at I/O address 51 Hex. The format of the interrupt control register is shown in Table 2.1. Writing a "1" to a specific bit position will enable that particular interrupt.

Table 2.1
INTERRUPT CONTROL/STATUS REGISTER
I/O ADDRESS 51 HEX CONTROL (WRITE)
I/O ADDRESS 50 HEX STATUS (READ)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1/MONTH	1/WEEK	1/DAY	1/HOUR	1/MIN	1/SEC	10/SEC	COMPARE

2.5.4. The status register located a I/O address 50 Hex is used to determine which source generated the interrupt, and to clear the interrupt by reading the status register. (The interrupt condition remains latched until cleared by reading the status register). The format of the interrupt status register is the same as the interrupt control register and is shown above in Table 2.1. Before enabling the interrupts, it is reccommended that the status register be read to clear any pending interrupts.

2.5.5. It should be noted that the interrupt generated by the MCM-CLK is a non-vectored, maskable interrupt. The CPU interrupts must be controlled accordingly to allow this interrupt scheme to work with the MCM-CLK. In particular, this type of interrupt scheme will not work with the Z80 mode 2 type interrupts. If the Z80 is to be used with the MCM-CLK in the interrupt mode, then the Z80 should be initialized for the mode 1 interrupt which will cause the processor to vector to location 38

Hex. At this point, the processor can poll the various interrupting devices to determine which device generated the interrupt.

2.6 EXAMPLES

2.6.1 The following section will give several examples of how to initialize and read the clock.

EXAMPLE #1
PROGRAMMING THE CLOCK

```
     LD   HL,TABLE  ;START ADDRESS OF INIT TABLE
     LD   B,08H     ;NUMBER OF BYTES TO TRANSFER
     LD   C,40H     ;OUTPUT PORT BASE ADDRESS
LOOP OUTI           ;OUTPUT (C)<--(HL)
     JP   Z,QUIT    ;IF Z=1 JUMP TO QUIT
     INC  C         ;INCREMENT OUTPUT PORT ADDRESS
     JP   LOOP      ;OUTPUT NEXT BYTE

TABLE:    DB   00   ;TEN THOUSANDTHS OF SECONDS
          DB   00   ;HUNDRETHS AND TENTHS OF SECONDS
          DB   00   ;SECONDS
          DB   30   ;MINUTES
          DB   13   ;HOURS
          DB   01   ;DAY OF WEEK
          DB   16   ;DAY OF MONTH
          DB   10   ;MONTH
```

THIS EXAMPLE WILL INITIALIZE THE CLOCK TO:

13:30:00:00:0, SUNDAY, 16 OCTOBER

EXAMPLE #2

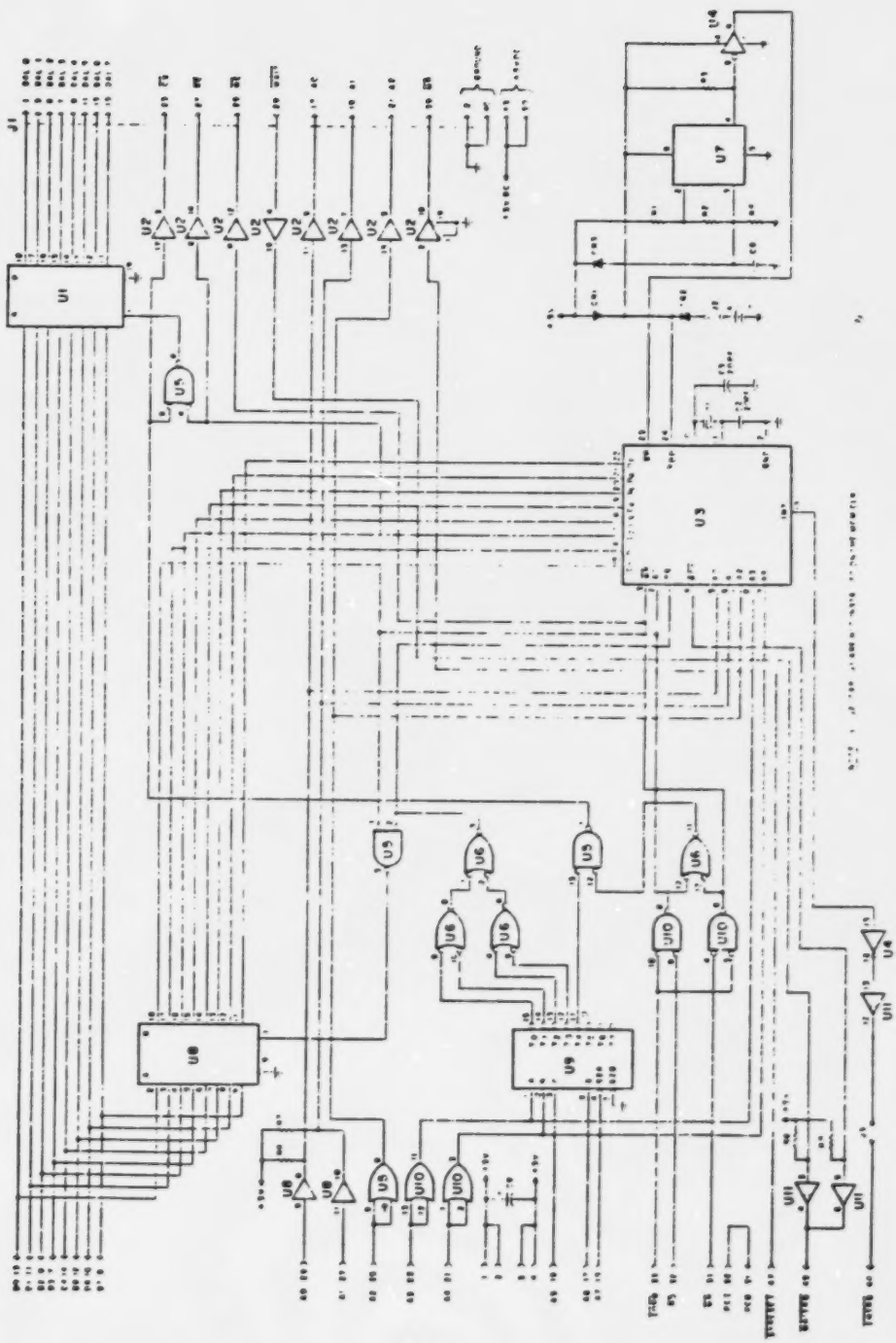
ROUTINE TO READ THE CLOCK

```
START:  LD   HL,TABLE   ;STARTING ADDRESS OF TABLE
        LD   B,08H      ;NUMBER OF BYTES TO READ
        LD   C,40H      ;STARTING ADDRESS
LOOP:   INI             ;READ (HL)<--(C)
        JP   Z,QUIT     ;IF Z=1 JUMP TO QUIT
        INC  C          ;INCREMENT INPUT PORT
        IN   A,(54H)    ;READ STATUS PORT
        CP   01         ;CHECK FOR ROLLOVER CONDITION
        JP   Z,START    ;REREAD COUNTERS IF Z=1
        JP   LOOP       ;READ ANOTHER BYTE


TABLE:  DS   1          ;1/10000  UPPER FOUR BITS
        DS   1          ;HUNDRETHS AND TENTHS OF SECONDS
        DS   1          ;SECONDS
        DS   1          ;MINUTES
        DS   1          ;HOURS
        DS   1          ;DAY OF WEEK
        DS   1          ;DAY OF MONTH
        DS   1          ;MONTH
```

MCM-CLK PARTS LIST

DESIGNATOR	DESCRIPTION
U3	MM58167A
U4	74HC04
U5,U10	74LS32
U6	74LS08
U7	8212CPA
U8	74LS245
U9	74LS138
U11	7407
C2,C3	20 PF MICA
C4-C8	.1UF
C9	22UF
R1	2.7K
R2	470 OHM
R3,R5-R8	15K
R4	1.1K
Y1	32,768HZ
X3	24 PIN SOCKET
B1	3.0V LITHIUM BATTERY
CR1-CR3	BAT47 DIODES



National Semiconductor

April 1982

MM58167A Microprocessor Real Time Clock

General Description

The MM58167A is a low threshold metal gate CMOS circuit that functions as a real time clock in bus oriented microprocessor systems. The device includes an addressable real time counter, 56 bits of RAM, and two interrupt outputs. A POWER DOWN input allows the chip to be disabled from the rest of the system for standby low power operation. The time base is a 32,768 Hz crystal oscillator.

Features

- Microprocessor compatible (8 bit data bus)
- 1/10,000 of a second through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- POWER DOWN input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32,768 Hz crystal oscillator
- Four year calendar (no leap year)
- 24 hour clock

Functional Description

Real Time Counter

The real time counter is divided into 4 bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table I. Any unused bits are held at a logical zero during a read and ignored during a write. An unused bit is any bit not necessary to provide a full BCD number. For example tens of hours cannot legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table I as dashes.

The addressable portion of the counter is from 1/10,000 of a second to months. The counter itself is a ripple counter. The ripple delay is less than 60 μs above 4.0V and 300 μs at 2.0V.

RAM

56 bits of RAM are contained on chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit ten thousandths of seconds and tens of days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones, then this RAM location will always compare.

The RAM is formatted the same as the real time counter, 4 bits per digit, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

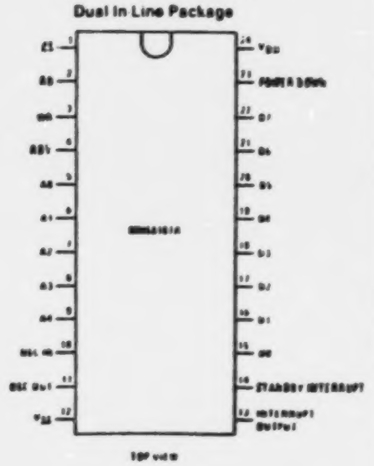
Interrupts and Comparator

There are two interrupt outputs. The first and most flexible is the INTERRUPT OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency (Figure 1). Once one or more bits have been set in the interrupt control register, the corresponding counter's rollover to its reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupting frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The second interrupt is the STANDBY INTERRUPT (open drain output, active low). This interrupt occurs when enabled and when a RAM/real time counter comparison occurs. The STANDBY INTERRUPT is enabled by writing a one on the D0 line at address $1E_H$ or disabled by writing a zero on the D0 line. This interrupt is not triggered by the edge of the compare signal, but rather by the level. Thus if the compare is enabled when the STANDBY INTERRUPT is enabled, the interrupt will turn on immediately.

Connection Diagram

Dual In Line Package



TOP VIEW

Absolute Maximum Ratings

Voltage at All Pins	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature	−40°C to 85°C
Storage Temperature	−65°C to 150°C
V_{DD}-V_{SS}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics V_{SS} = 0V, −40°C ≤ T_A ≤ 85°C

Parameter	Conditions	Min	Max	Units
Supply Voltage				
V_{DD}	Outputs Enabled	4.0	5.5	V
V_{DD}	POWER DOWN Mode	2.0	5.5	V
Supply Current				
I_{DD} Static	Outputs TRI-STATE®			
	f_{IN} = DC, V_{DD} = 5.5V		10	μA
I_{DD} Dynamic	Outputs TRI-STATE			
	f_{IN} = 32 kHz, V_{DD} = 5.5V			
	V_{IH} = V_{DD} − 0.3V			
	V_{IL} = V_{SS} + 0.3V		20	μA
I_{DD} Dynamic	Outputs TRI-STATE			
	f_{IN} = 32 kHz, V_{DD} = 5.5V			
	V_{IH} = 2.0V, V_{IL} = 0.8V		5	mA
Input Voltage				
Logical Low		0.0	0.8	V
Logical High		2.0	V_{DD}	V
Input Leakage Current	V_{SS} < V_{IN} < V_{DD}	−1	1	μA
Output Impedance	I/O and INTERRUPT OUT			
Logical Low	V_{DD} = 4.5V, I_{OL} = 1.6 mA		0.4	V
Logical High	V_{DD} = 4.5V, I_{OH} = −400 μA	2.4		V
	I_{OH} = −10 μA	0.8 V_{DD}		V
TRI-STATE	V_{SS} < V_{out} < V_{DD}	−1	1	μA
Output Impedance	RDY and STANDBY INTERRUPT			
Logical Low Sink	V_{out} = 4.5V, I_{OL} = 1.6 mA		0.4	V
Logical High Leakage	V_{out} < V_{DD}		10	μA

Functional Description (Continued)

TABLE I. REAL TIME COUNTER FORMAT

Counter Addressed		Units D0	D1	D2	D3	Max BCD Code	Tens D4	D5	D6	D7	Max BCD Code
1/10,000 of Seconds	(00_H)	-	-	-	-	0	D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01_H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02_H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Minutes	(03_H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Hours	(04_H)	D0	D1	D2	D3	9	D4	D5	-	-	2
Day of the Week	(05_H)	D0	D1	D2	-	7	-	-	-	-	0
Day of the Month	(06_H)	D0	D1	D2	D3	9	D4	D5	-	-	3
Month	(07_H)	D0	D1	D2	D1	9	D4	-	-	-	1

(-) Indicates unused bits.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Functional Description (Continued)

TABLE II ADDRESS CODES AND FUNCTIONS

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter – Ten Thousandths of Seconds
0	0	0	0	1	Counter – Hundredths and Tenths of Seconds
0	0	0	1	0	Counter - Seconds
0	0	0	1	1	Counter - Minutes
0	0	1	0	0	Counter - Hours
0	0	1	0	1	Counter - Day of Week
0	0	1	1	0	Counter - Day of Month
0	0	1	1	1	Counter - Month
0	1	0	0	0	RAM - Ten Thousandths of Seconds
0	1	0	0	1	RAM - Hundredths and Tenths of Seconds
0	1	0	1	0	RAM - Seconds
0	1	0	1	1	RAM - Minutes
0	1	1	0	0	RAM - Hours
0	1	1	0	1	RAM - Day of Week
0	1	1	1	0	RAM - Day of Month
0	1	1	1	1	RAM - Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counters Reset
1	0	0	1	1	RAM Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	GO Command
1	0	1	1	0	STANDBY INTERRUPT
1	1	1	1	1	Test Mode

All others unused

Functional Description (Continued)

The comparator is a cascaded exclusive NOR. Its output is latched 61 μs after the rising edge of the 1 kHz clock signal (input to the ten thousandths of seconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.0V the thousandths of seconds counter should not be included in a compare because of the possibility of having a ripple delay greater than 61 μs. (For output timing see Interrupt Timing.)

Power Down Mode

The POWER DOWN input is essentially a second chip select. It disables all inputs and outputs except for the STANDBY INTERRUPT. When this input is at a logical zero, the device will not respond to any external signals. It will however maintain timekeeping and turn on the STANDBY INTERRUPT if programmed to do so. (The programming must be done before the POWER DOWN input goes to a logical zero.) When switching V_{DD} to the standby or power down mode, the POWER DOWN input should go to a logical zero at least 1 μs before V_{DD} is switched. When switching $V_{(d)}$ all other inputs must remain between V_{SS} − 0.3V and V_{DD} + 0.3V. When restoring V_{DD} to the normal operating mode it is necessary to ensure that all other inputs are at valid levels before switching the POWER DOWN input back to a logical one. These precautions are necessary to insure that no data is lost or altered when changing to or from the power down mode.

Counter and RAM Resets, GO Command

The counters and RAM can be reset by writing all 1's (F's) at address 12_H or 13_H respectively.

A write pulse at address 15_H will reset the thousandths, hundredths, tenths, units, and tens of seconds counters. The GO command is used for precise starting of the clock. The data on the data bus is ignored during the write. If the seconds counter is at a value greater than 40 when the GO is issued, the minute counter will increment; otherwise the minute counter is unaffected. This command is not necessary to start the clock, but merely a convenient way to start precisely at a given minute. (See Table III for reset format.)

Status Bit

The status bit is provided to inform the user that the clock is in the process of rolling over when a counter is read. The 1 kHz clock into the thousandths of seconds counter has a pulse width of 61 μs. If a read of the real time counter (any digits) is done during this 61 μs period the status bit will be set. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be reread.

The status bit appears on D0 when address 14_H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or series of counter reads are done. The trailing edge of the read at address 14_H will reset the status bit.

Oscillator

The oscillator used is the standard Pierce oscillator. Externally only 2 capacitors and the crystal are required. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200 kΩ. The capacitor values should be typically 20 pF - 25 pF. The crystal frequency is 32.768 kHz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input levels should be within 0.3V of the supplies.

A ground line or ground plane between pins 9 and 10 may be necessary to prevent interference of the oscillator by the A4 address.

Control Lines

The READ, WRITE, and CHIP SELECT signals are active low inputs. The READY signal is an open drain output. At the start of each read or write cycle the READY line (open drain) will pull low and will remain low until valid data from a chip read appears on the bus or data on the bus is latched in during a write. READ and WRITE must be accompanied by a CHIP SELECT (see *Figures 3* and *4* for read and write cycle timing).

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 kHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at $1F_H$.

Functional Description (Continued)

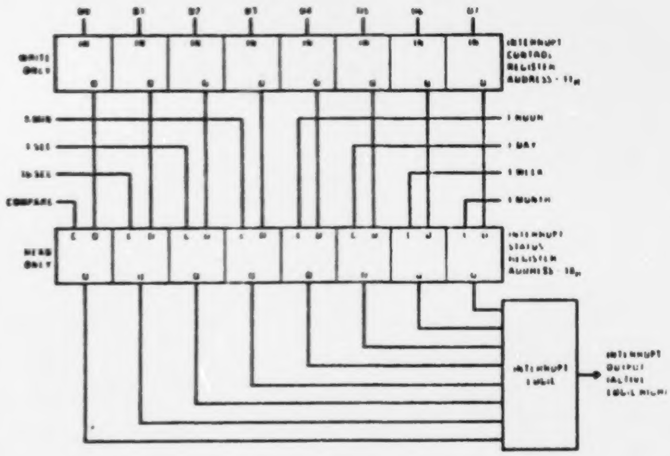


FIGURE 1 Interrupt Register Format

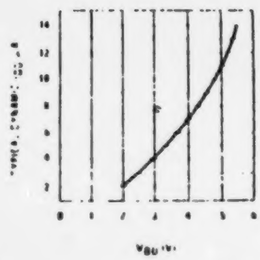


FIGURE 2 Typical Supply Current vs Supply Voltage

Interrupt Timing $-40^{\circ}C \le T_A \le 85^{\circ}C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

Parameter		Min	Max	Units
t_{INTON}	Status Register Clock to INTERRUPT OUTPUT (Pin 13) High (Note 1)		5	µS
t_{SBYON}	Compare Valid to $\overline{\text{STANDBY INTERRUPT}}$ (Pin 14) Low (Note 1)		5	µS
t_{INTOFF}	Trailing Edge of Status Register Read to INTERRUPT OUTPUT Low		5	µS
t_{SBYOFF}	Trailing Edge of Write Cycle (D0 = 0; Address = 16_H) to $\overline{\text{STANDBY INTERRUPT}}$ Off (High Impedance State)		5	µS

Note 1: The status register clocks are the corresponding counter's rollover to its reset state or the compare becoming valid. The compare becomes valid 61 µs after the 1/10,000 of a second counter is clocked, if the real time counter data matches the RAM data.

Read Cycle Timing $-40^{\circ}C \le T_A \le 85^{\circ}C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

Parameter		Min	Max	Units
t_{AR}	Address Bus Valid to Read Strobe	100		ns
t_{CSR}	Chip Select to Read Strobe	0		ns
t_{RRY}	Read Strobe to Ready Strobe		150	ns
t_{RYD}	Ready Strobe to Data Valid		800	ns
t_{AD}	Address Bus Valid to Data Valid		1050	ns
t_{RH}	Data Hold Time From Trailing Edge of Read Strobe	0		ns
t_{HZ}	Trailing Edge of Read Strobe to TRI-STATE Mode		250	ns
t_{RYH}	Read Hold Time after Ready Strobe	0		ns
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	50		ns

Note 2: If $t_{AR} = 0$ and $t_{RRY} = 0$ and Chip Select, Address Valid, Read or Write are coincident then they must exist for 1050 ns.

Write Cycle Timing - $-40°C \le T_A \le 85°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

	Parameter	Min	Max	Units
t_{AW}	Address Valid to Write Strobe	100		ns
t_{CSW}	Chip Select to Write Strobe	0		ns
t_{DW}	Data Valid before Write Strobe	100		ns
t_{WRY}	Write Strobe to Ready Strobe		150	ns
t_{RY}	Ready Strobe Width		800	ns
t_{WHY}	Write Hold Time after Ready Strobe	0		ns
t_{WD}	Data Hold Time after Write Strobe	110		ns
t_{WA}	Address Hold Time after Write Strobe	50		ns

Data Bus loading is 100 pF

Ready Output loading is 50 pF and 20 kΩ pull up

Input and output AC timing levels

Logical one = 2.0V

Logical zero = 0.8V

Read and Write Cycle Timing Diagrams

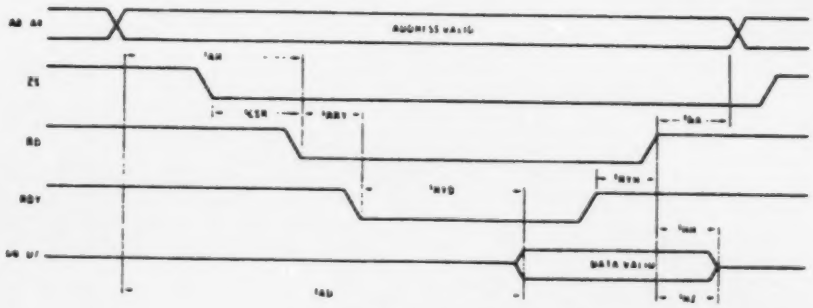


FIGURE 3 Read Cycle Timing

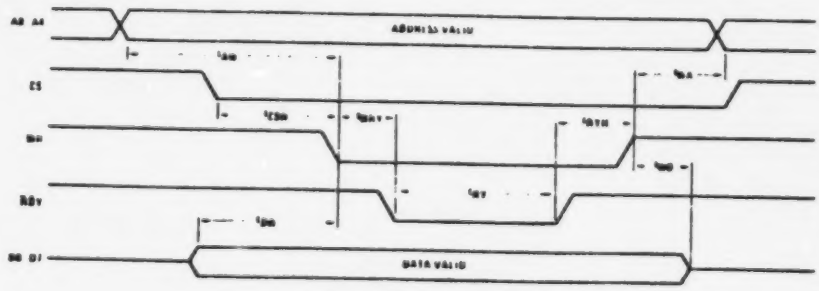


FIGURE 4. Write Cycle Timing

Typical Applications

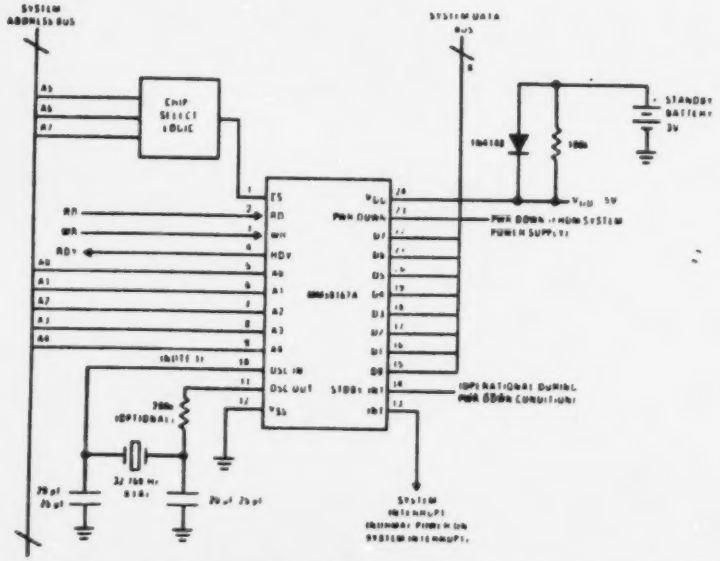


FIGURE 5. Typical Connection Diagram

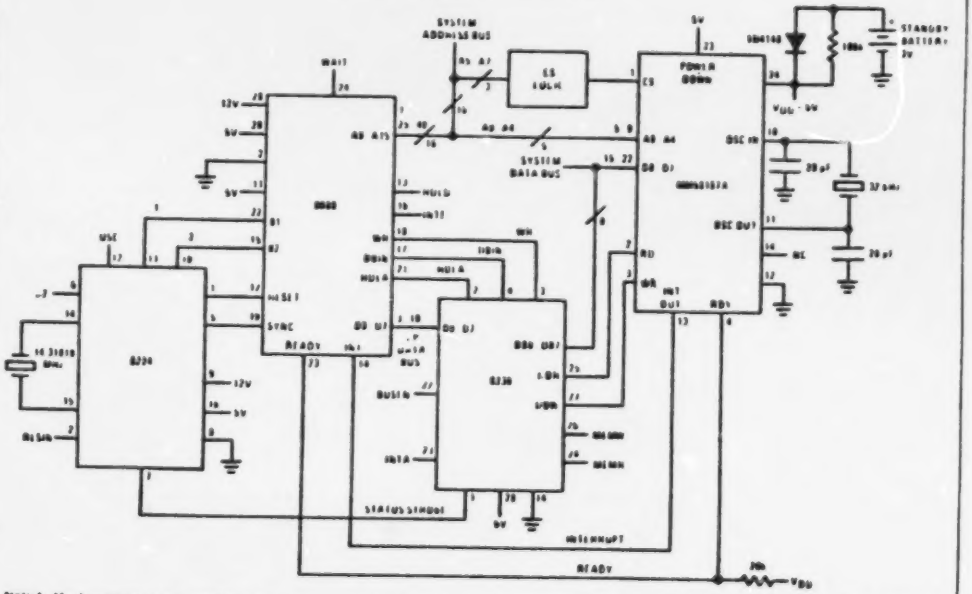


FIGURE 6. 8080 System Interface with Battery Backup

Block Diagram

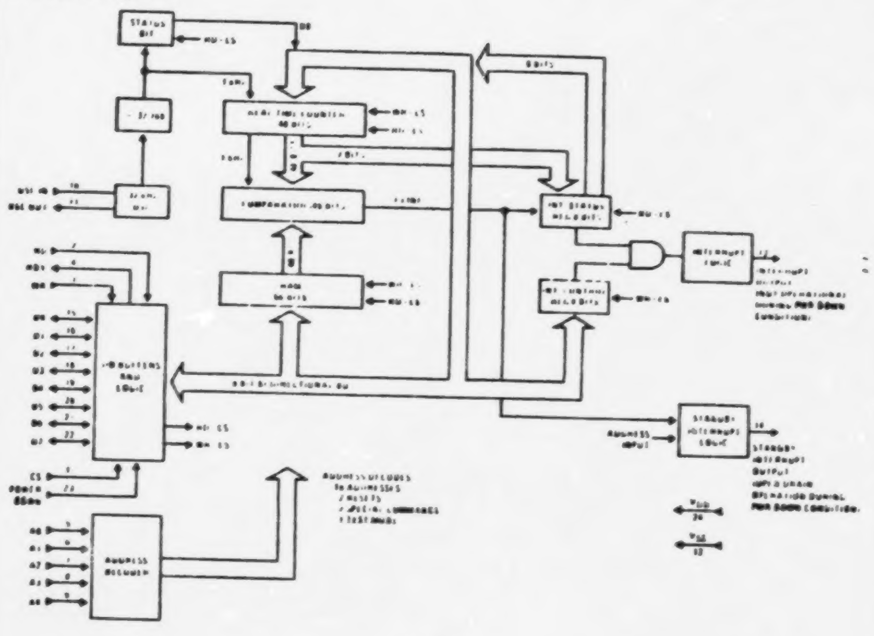


FIGURE 7

Physical Dimensions inches (millimeters)

Molded Dual In Line Package (N)
Order Number MM58167AN
NS Package Number N24A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

APPENDICE G

CARTE DE COMMUNICATION (73C04)

CRIQ

PRO-LOG CORPORATION

STD 7000

73C04
CMOS Dual UART Card

USER'S MANUAL

3/84

FOREWORD

This manual explains how to use Pro-Log's 73C04 CMOS dual UART (Universal Asynchronous Receiver/Transmitter) card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 73C04. We welcome your suggestions on how we can improve our instructions.

The 73C04 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of using his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: the **Microprocessor User's Guide** and the **Series 7000 STD BUS Technical Manual**. If you would like a copy of these publications, please submit your request on your company letterhead.

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SECTION 1
Purpose and Main Features

PURPOSE

The 73C04 is a general purpose serial data communications card for STD CMOS systems. It provides two fully independent RS-232-C serial data communication channels on a single card which may be inserted in any slot on an STD BUS card rack system. Asynchronous operation up to 19200 baud is provided for full duplex DTE (Data Terminal Equipment) or DCE (Data Communications Equipment) applications.

The card is shipped with eight software-selectable baud rates. However, if a specific application requires alternate baud rates, two optional sets are available by simply changing on-card jumpers.

The 73C04 has polled interrupt logic for both channels. If priority interrupt logic is desired, a connection is available (e.g., the restart interrupt pins on an 80C85A).

FEATURES

- CMOS wide temperature range, high noise immunity, and low power characteristics
- Conforms to RS-232-C serial interface specification
- Dual, independent CMOS 82C51A UARTs
- Independent program-selectable baud rates to 9600 baud for RS-232-C
- Baud rates to 19200 by jumper selection
- Independent polled interrupt logic
- External interrupts are provided on a user connector
- Selectable DTE/DCE configuration for each channel
- Dual 26-pin male header connectors for RS-232-C interface
- +5V, ±12V operation
- CMOS Z80 and 80C85 processor capability

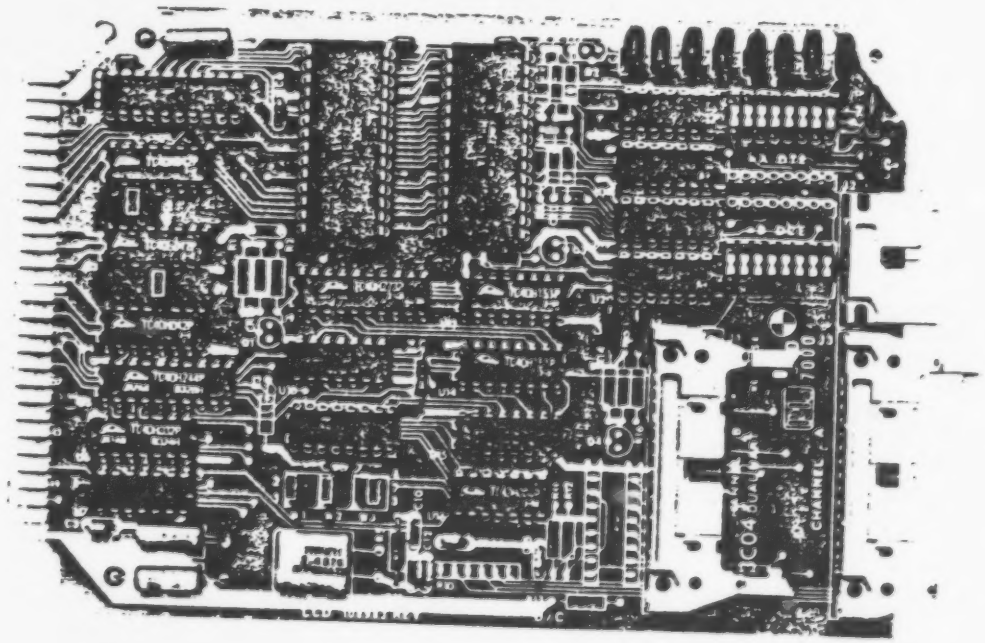


Figure 1-1. 73C04 CMOS Dual UART Card

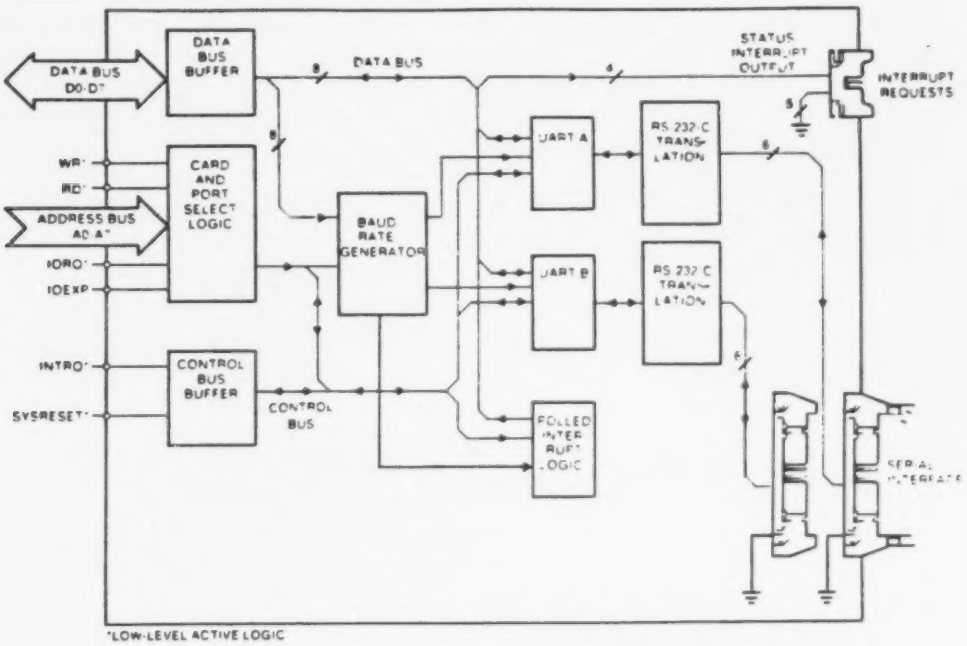


Figure 1-2. 73C04 Block Diagram

SECTION 2
Installation and Specifications

INTRODUCTION

This section explains the functions and options of the 73C04 card which should be considered before the card is installed in your system. This section also covers the product specifications.

PRODUCT NOTICE

To guarantee the proper operation of the 73C04 CMOS dual UART card, care must be taken to ensure that the LOGIC GND and AUX GND are connected at the user's power supply.

Pro-Log power supplies are shipped with both GNDs bused together and therefore meet these requirements. If a source other than Pro-Log is used for power supplies, then care must be taken to ensure that these requirements are met.

The 73C04 CMOS dual UART card is composed of CMOS parts, and is intended to be used only in CMOS card systems.

INSTALLATION

CAUTION

CMOS integrated circuits must be protected from electrostatic discharge. Use conductive foam pads or conductive plastic bags, and never place CMOS circuitry in contact with styrofoam materials.

The 73C04 card operates as part of a CMOS STD BUS card rack system.

The 73C04 can be inserted in any slot in the card rack. Power should be off, and it should be inserted with the card ejector tab at the top of the card (see figure 2-1).

CAUTION

To prevent possible damage to the STD BUS system, make sure that power is off before inserting a card into the card rack, or before removing a card from the card rack.

If access to the card is needed, it can be installed in either end of an open-ended card rack, or in a card extender such as the Pro-Log 7901. The card extender may be inserted in any slot in the card rack and the 73C04 inserted in the card extender.

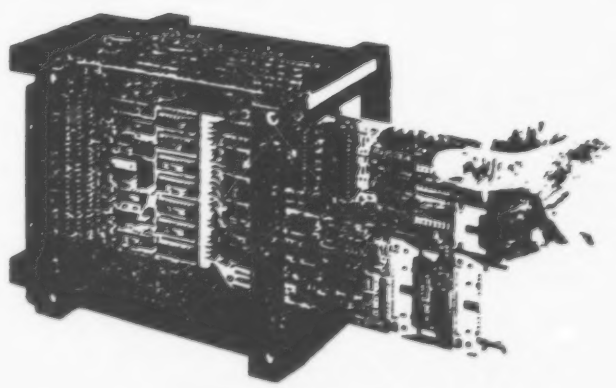


Figure 2-1. Installation of 73C04 Card

RS-232-C INTERFACE CONNECTIONS

The serial communication connectors (J1 and J3) are latching 26-pin headers. When using the 73C04 for RS-232-C serial communication, a Pro-Log RC701, RC702, or similar interconnect cable will be needed to convert the 26-pin transition connector to a standard D connector with pinouts meeting the RS-232-C Specification (see figure 2-14). The RC701 cable provides a male 25-pin D connector and the RC702, a female 25-pin D connector.

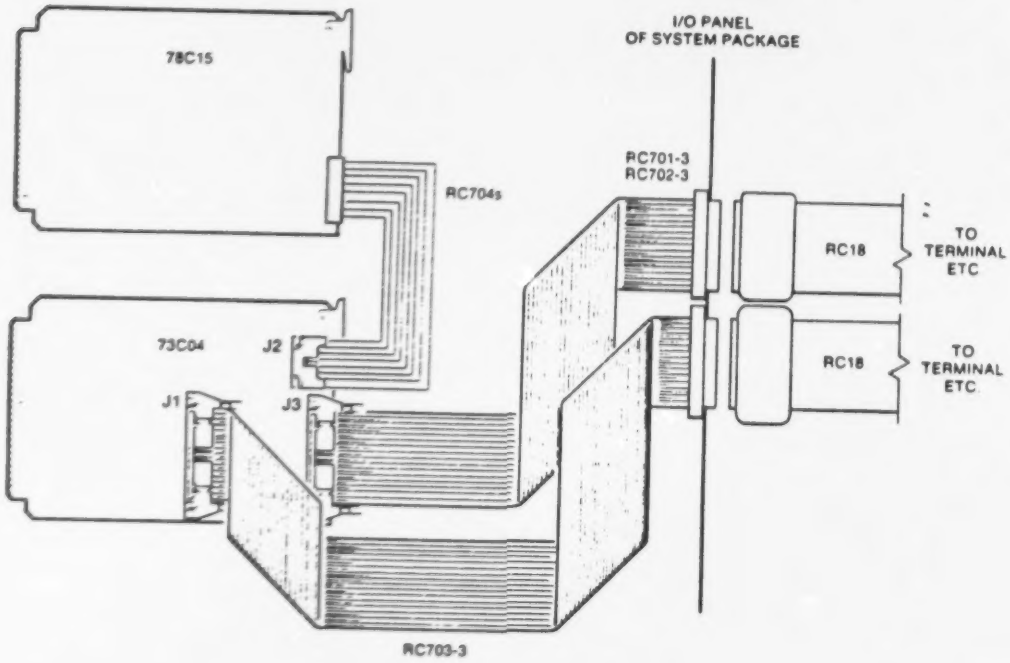


Figure 2-2. 73C04 Cabling Example

Pro-Log also offers the RC18 cable which incorporates a male 25-pin D connector on one end and a female 25-pin D connector on the other. This cable can be used as an extension connection between your terminal and the RC701 or RC702.

INTERRUPT INTERFACE CONNECTOR

The 73C04 also contains an interrupt interface connector. This connector is a 10-pin header (J2) with alternating signal and ground lines.

A Pro-Log RC704 interconnect cable (twisted cable pair for noise immunity) may be used to connect individual interrupt lines to prioritized interrupts on a CMOS CPU card.

I/O MAPPED CARD ADDRESSING

The 73C04's input and output ports respond to single read and write instructions executed in the processor's operating program. The 73C04 is enabled when a jumper-selected combination of address lines A0 through A7 is present, and when the following control lines are active: IORQ*, IOEXP, and either RD* or WR*.

The 73C04 provides eight consecutive I/O addresses regardless of its mapping assignment and is shipped with standard mapping to port addresses E0 through E7. These preferred addresses allow easy adaptation of standard Pro-Log software. These addresses may be retained, or can be changed with jumpers SX and SY (see figures 2-3 and 2-4). The port addresses on this card are arbitrary, however, they must differ from all other I/O port addresses in the system. If they do not differ, multiple cards will respond to the same Read instruction, resulting in bus contention.

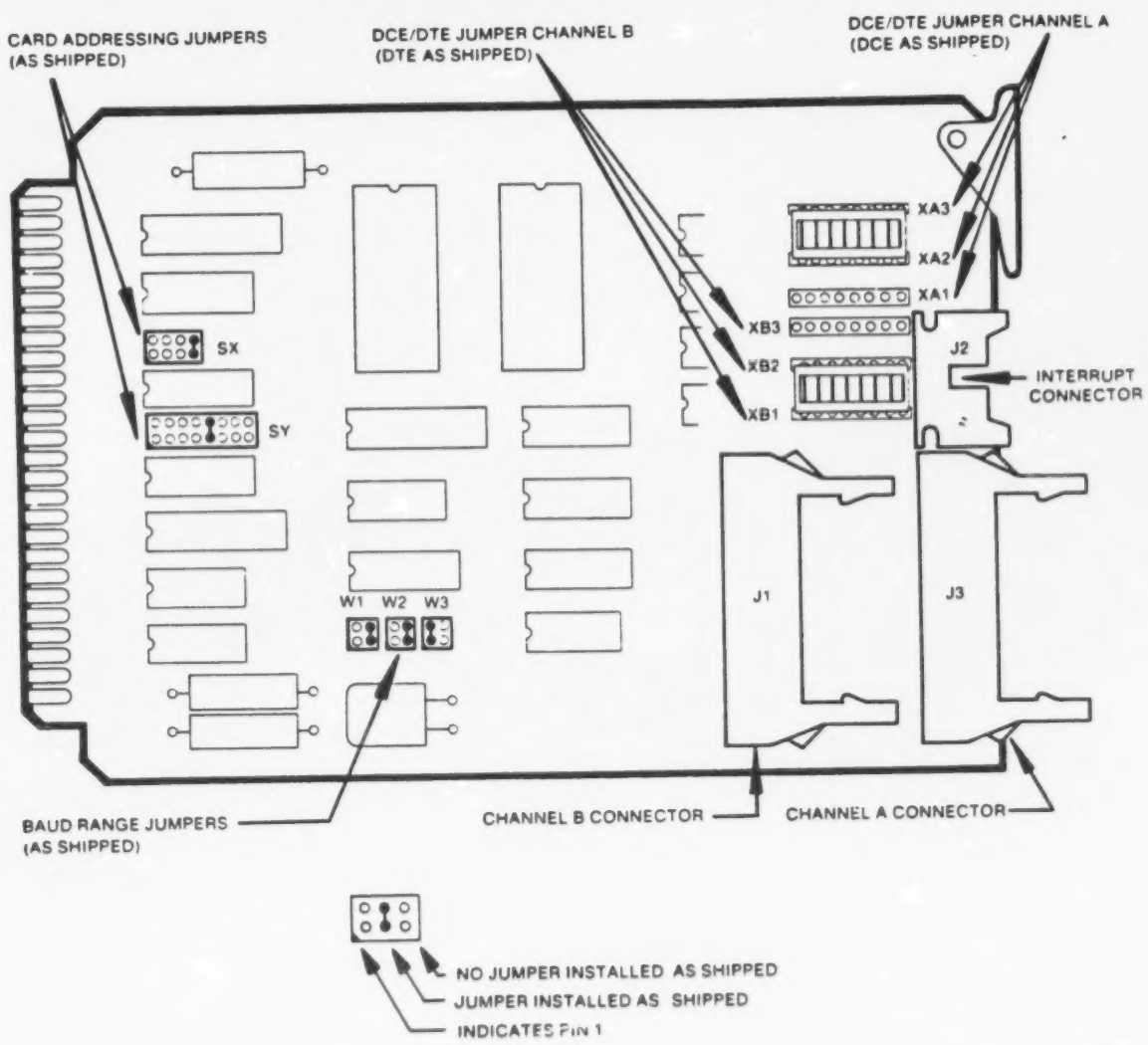


Figure 2-3. 73C04 Physical Location of Components

CHANGING THE PORT ADDRESSES

The 73C04 can be remapped anywhere within a 256 port addressing range. To change the I/O addressing of the 73C04, change jumpers SX and SY. Figure 2-3 shows these jumper locations and figure 2-4 shows the jumper positions required for alternate mapping of the 73C04.

PORTS	JUMPERS
00	SX0
01	
02	
03	
04	SY0
05	
06	
07	
08	SX0
09	
0A	
0B	
0C	SY1
0D	
0E	
0F	
10	SX0
11	
12	
13	
14	SY2
15	
16	
17	
18	SX0
19	
1A	
1B	
1C	SY3
1D	
1E	
1F	
20	SX0
21	
22	
23	
24	SY4
25	
26	
27	
28	SX0
29	
2A	
2B	
2C	SY5
2D	
2E	
2F	
30	SX0
31	
32	
33	
34	SY6
35	
36	
37	
38	SX0
39	
3A	
3B	
3C	SY7
3D	
3E	
3F	

PORTS	JUMPERS
40	SX1
41	
42	
43	
44	SY0
45	
46	
47	
48	SX1
49	
4A	
4B	
4C	SY1
4D	
4E	
4F	
50	SX1
51	
52	
53	
54	SY2
55	
56	
57	
58	SX1
59	
5A	
5B	
5C	SY3
5D	
5E	
5F	
60	SX1
61	
62	
63	
64	SY4
65	
66	
67	
68	SX1
69	
6A	
6B	
6C	SY5
6D	
6E	
6F	
70	SX1
71	
72	
73	
74	SY6
75	
76	
77	
78	SX1
79	
7A	
7B	
7C	SY7
7D	
7E	
7F	

PORTS	JUMPERS
80	SX2
81	
82	
83	
84	SY0
85	
86	
87	
88	SX2
89	
8A	
8B	
8C	SY1
8D	
8E	
8F	
90	SX2
91	
92	
93	
94	SY2
95	
96	
97	
98	SX2
99	
9A	
9B	
9C	SY3
9D	
9E	
9F	
A0	SX2
A1	
A2	
A3	
A4	SY4
A5	
A6	
A7	
A8	SX2
A9	
AA	
AB	
AC	SY5
AD	
AE	
AF	
B0	SX2
B1	
B2	
B3	
B4	SY6
B5	
B6	
B7	
B8	SX2
B9	
BA	
BB	
BC	SY7
BD	
BE	
BF	

PORTS	JUMPERS
C0	SX3
C1	
C2	
C3	
C4	SY0
C5	
C6	
C7	
C8	SX3
C9	
CA	
CB	
CC	SY1
CD	
CE	
CF	
D0	SX3
D1	
D2	
D3	
D4	SY2
D5	
D6	
D7	
D8	SX3
D9	
DA	
DB	
DC	SY3
DD	
DE	
DF	
E0	SX3
E1	
E2	
E3	
E4	SY4
E5	
E6	
E7	
E8	SX3
E9	
EA	
EB	
EC	SY5
ED	
EE	
EF	
F0	SX3
F1	
F2	
F3	
F4	SY6
F5	
F6	
F7	
F8	SX3
F9	
FA	
FB	
FC	SY7
FD	
FE	
FF	

Shading denotes as-shipped configuration.

Figure 2-4. Jumpers Required for 73C04 Port Address Mapping

JUMPERS

73C04 optional functions are selected by connecting permanent 0.025-inch square post headers with slip-on, slip-off connectors.

DCE/DTE RS-232-C Configuration

When using the RS-232-C interface on channels A or B, first determine whether the card is used as DTE (data terminal equipment), a terminal, or as DCE (data communications equipment), a modem. As shipped, the 73C04 has channel A configured for DCE and channel B configured for DTE (see figure 2-3). To reconfigure the 73C04, change the 16-pin programming headers.

To select a particular mode, install the header in the correct sockets indicated on the card. The header should cover the silkscreen on the card when installed properly. For example, to configure channel A as DCE, place the header in XA3 and XA2, covering "A DCE" (figure 2-3).

BAUD RATE RANGE JUMPERS

The 73C04 is shipped with eight software-selectable baud rates available to the user. If the baud rate required is not one of these eight, on-card jumpers W1, W2, and W3 can be changed to select alternate sets of baud rates. Figure 2-3 locates these jumpers, and figure 2-5 shows which baud rates are available for each range. Figure 2-6 shows the jumpers to be connected for each baud range. Section 3 explains the software for selecting one of the eight baud rates within the range.

TERMINATION

Since the input impedance of CMOS is very large, the main restriction on fanout is load capacitance. As the total capacitive load on an output is increased, the propagation delays increase, along with power consumption. Since Pro-Log's 7909A termination network card and 7106 motherboard use termination that present large capacitive loads, these products should not be used with CMOS cards. Check any other termination in the system for capacitive loading and power dissipation.

Baud No.	Baud Rate As Shipped	Baud Rate Option 1	Baud Rate Option 2
16X Baud Rate Factor[1]			
0	110	75	2400
1	150	0	600
2	300	0	200
3	1200	0	75
4	1800	50	50
5	2400	0	134.5
6	4800	19200	0
7	9600	19200	0
64X Baud Rate Factor[1]			
0	27.5	18.75	600
1	37.5	0	150
2	75	0	50
3	300	0	18.75
4	450	12.5	12.5
5	600	0	33.63
6	1200	4800	0
7	2400	4800	0

[1] The 16X or 64X baud rate factor is a software-selectable function explained in section 3 of this manual.

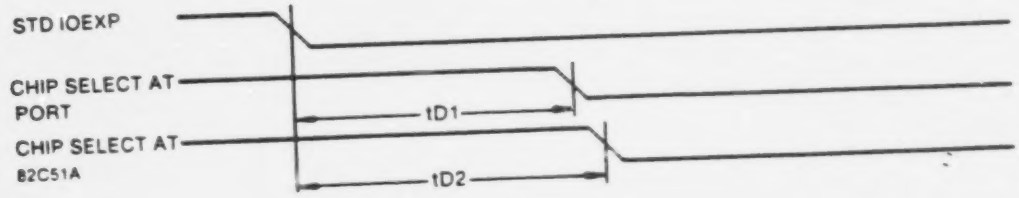
Figure 2-5. 73C04 Baud Rate Options

Baud Rate Option	W1		W2		W3	
	1-2	3-4	1-2	3-4	1-2	3-4
As Shipped	Open	Shorted	Open	Shorted	Shorted	Open
Option 1	Shorted	Open	Shorted	Open	Open	Shorted
Option 2	Open	Shorted	Open	Shorted	Open	Shorted

Figure 2-6. 73C04 Baud Range Jumper Table

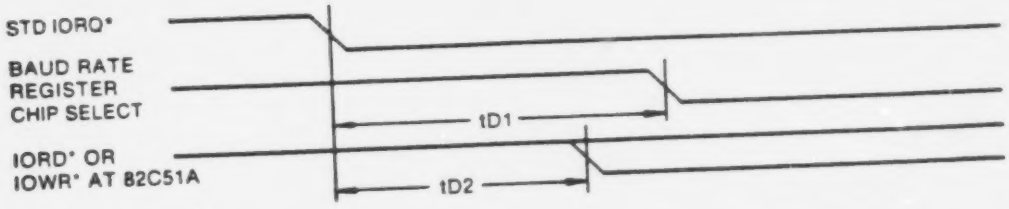
TIMING

73C04 STD BUS timing and the effect of each specific signal on the 73C04 card is shown in figures 2-7 through 2-13. The signals as shown assume all other signals are valid before they become valid. These timing charts are independent of CPU card timing.



SYMBOL	PARAMETER	NANOSECONDS TYP	NANOSECONDS MAX
tD1	Time IOEXP low to chip select low at Baud Rate Register	154	231
tD2	Time IOEXP low to chip select at 82C51A low	155	233

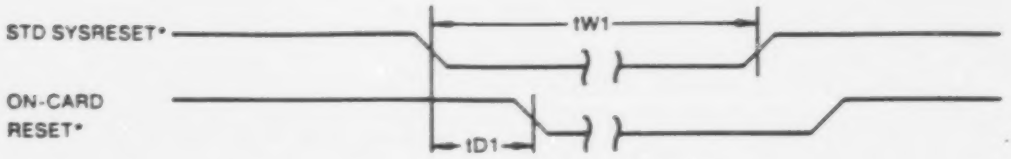
Figure 2-7. IOEXP Timing



SYMBOL	PARAMETER	NANOSECONDS TYP	NANOSECONDS MAX
tD1	Time IORQ* low to chip select low at Baud Rate Register	64	96
tD2	Time IORQ* low until RD* and WR* signals are enabled at 82C51A (see note)	46	69

Note: The STD RD* and WR* signals are only gated through to the 82C51A when IORQ* is low. The RD* and WR* lines at the 82C51A are always high when IORQ* is high.

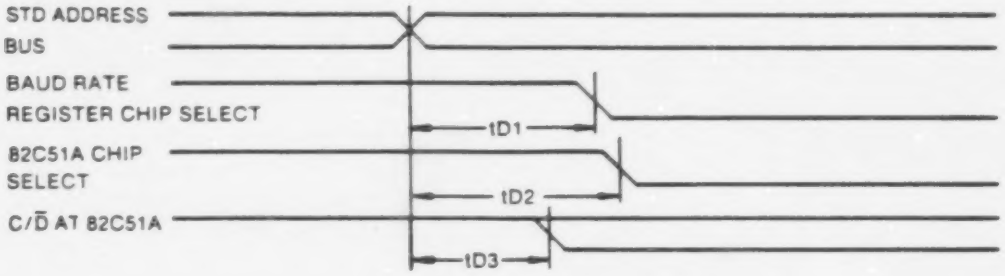
Figure 2-8. IORQ* Timing



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
tD1	Time SYSRESET* low until Reset* low at output port		28	42	ns
tW1	Minimum reset pulse width allowed (see note)	6 tcy			μs

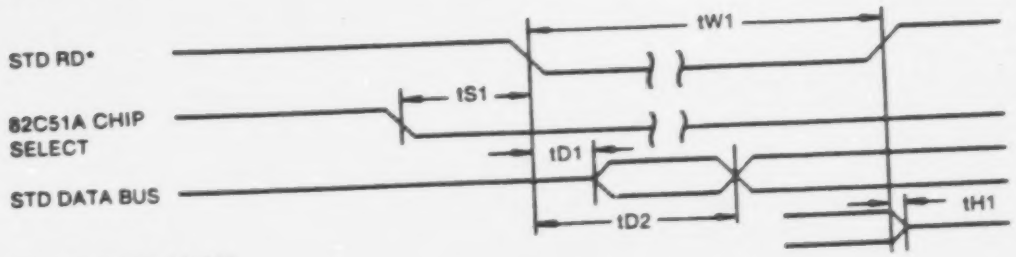
Note: tcy = clock period = 1/Baud Rate

Figure 2-9. Reset Timing



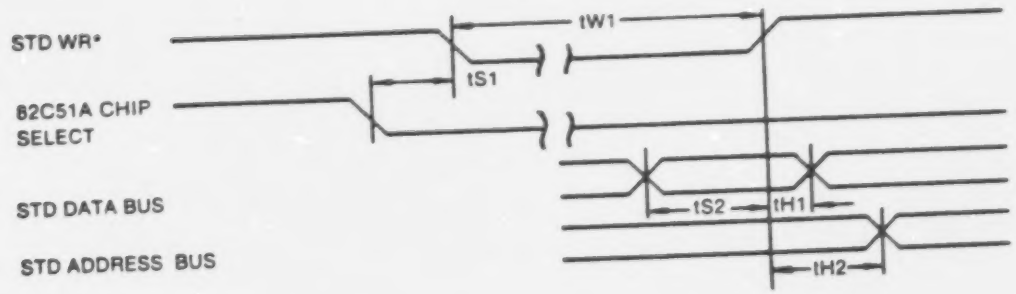
SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tD1	Time address valid until Baud Rate Register chip select low	126	189
tD2	Time address valid until 82C51A chip select low	127	191
tD3	Time address valid until C/D̄ valid at 82C51A	108	162

Figure 2-10. Address Access Time



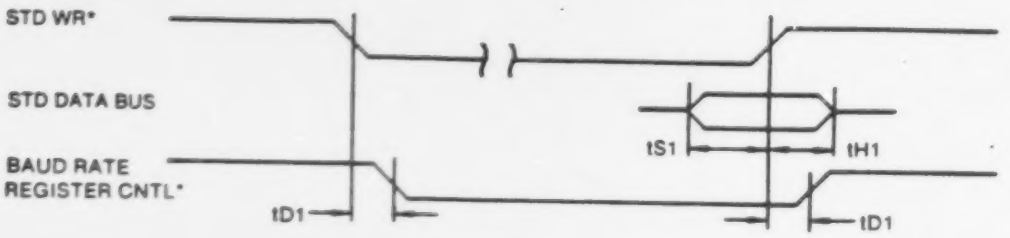
SYMBOL	PARAMETER	NANOSECONDS MIN	TYP	MAX
tD1	Time RD* low until data bus driven		46	69
tD2	Time RD* low until data bus valid		269	304
tH1	Minimum address hold time allowed after RD* high	104		
tS1	Minimum chip select setup time allowed	0		
tW1	Minimum RD* pulse width allowed	250		

Figure 2-11. Read Timing for 82C51A



SYMBOL	PARAMETER	NANOSECONDS MIN	TYP	MAX
tH1	Minimum data hold time	35		
tH2	Minimum address hold time	69		
tS1	Minimum chip select setup time allowed	0		
tS2	Minimum data setup time allowed	185		
tW1	Minimum WR* pulse width allowed	250		

Figure 2-12. 73C04 Write Timing for 82C51A



SYMBOL	PARAMETER	NANOSECONDS		
		MIN	TYP	MAX
tD1	Time WR* until Baud Rate Register CNTL* high or low		64	96
tH1	Minimum data hold time	96		
tS1	Minimum data setup time	0		

Figure 2-13. 73C04 Write Timing for Baud Rate Register

73C04 USER INTERFACE CONNECTORS

Figures 2-14 through 2-17 show pinouts for the RC701 and RC702 cables when used with the signal flow from the 73C04 card to the interfacing equipment in the DCE and DTE configurations. Figures 2-19 and 2-20 show the part numbers of compatible cables and connectors.

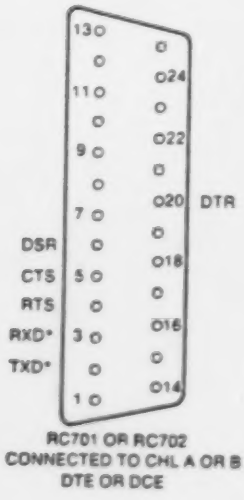


Figure 2-14. RC701 and RC702 Pinouts When Connected to 73C04

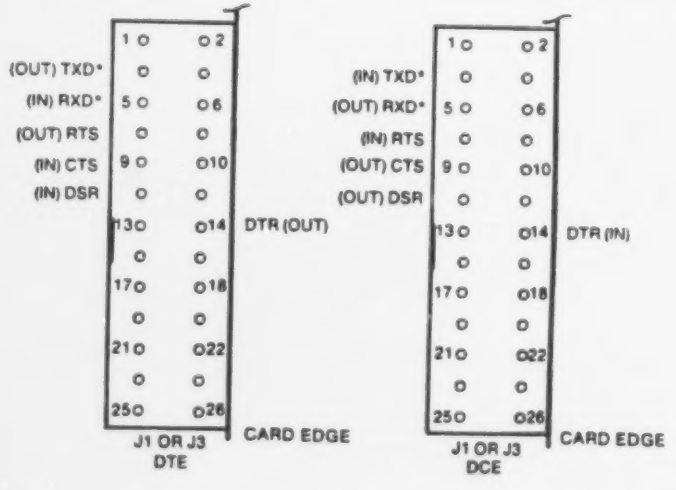


Figure 2-15. 73C04 J1 and J3 Pinouts

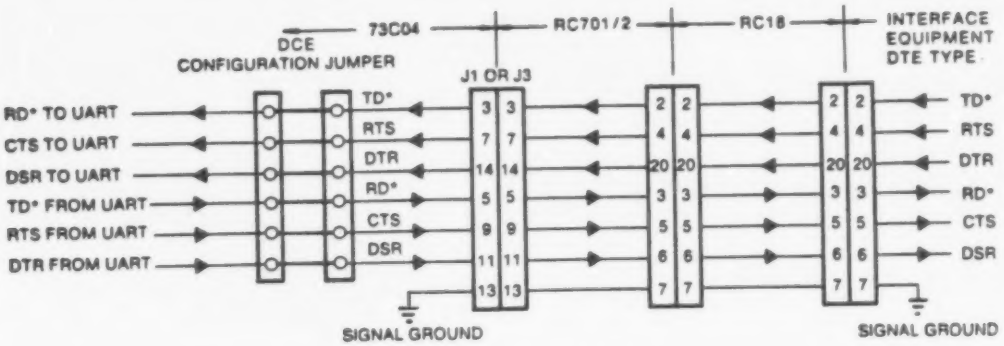


Figure 2-16. 73C04 Signal Flow in DCE Configuration

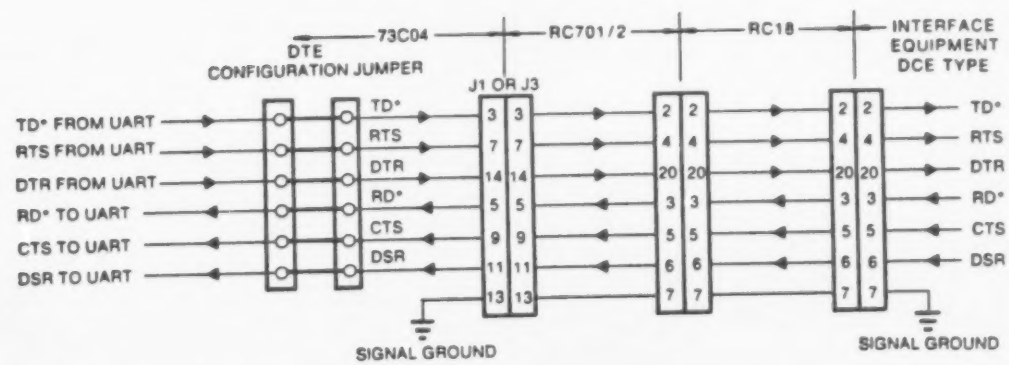


Figure 2-17. 73C04 Signal Flow in DTE Configuration

MECHANICAL SPECIFICATIONS

The 73C04 meets all general mechanical specifications of the STD BUS.

PIN NUMBER SIGNAL FLOW SIGNAL		PIN NUMBER	PIN NUMBER SIGNAL FLOW SIGNAL	
TRANSMITTER A READY	OUT 2	1		GROUND
RECEIVER A READY	OUT 4	3		GROUND
TRANSMITTER B READY	OUT 6	5		GROUND
RECEIVER B READY	OUT 8	7		GROUND
NOT CONNECTED	— 10	9		GROUND

Figure 2-18. 73C04 Interrupt Interface Connector J2

CABLE	USE AND DESCRIPTION
RC701-3	73C04 to Male 25-pin D connector (RS-232-C)
RC702-3	73C04 to Female 25-pin D connector (RS-232-C)
RC18	Female 25-pin D to Male 25-pin D (RS-232-C)
RC704	Two wire twisted pair for use with interrupt connector. Can connect to all 73C04 interface connectors.

Figure 2-19. Pro-Log Cables for Use with 73C04

MFG	26-PIN CONNECTOR FOR J1 AND J3	10-PIN CONNECTOR FOR J2
Berg	65823-073	65496-001
SAE	RH6226D2RLS	RP6210D2RH
3M	3429-1302	3491-1002

NOTE: This list is provided for customer convenience. Many other manufacturer's connectors are compatible. For more information consult manufacturers' catalogs.

Figure 2-20. 73C04 Compatible Connectors

ENVIRONMENTAL SPECIFICATIONS

PARAMETER	Recommended Operating Limits			Absolute Nonoperating Limits		
	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	-40	25	+85	-40	+100	°C
Noncondensing Relative Humidity	5		95	0	95	%RH

Figure 2-21. 73C04 Environmental Specifications

ELECTRICAL SPECIFICATIONS

PARAMETER	Recommended Operating Limits			Absolute Nonoperating Limits		
	MIN	TYP	MAX	MIN	MAX	UNITS
VCC	4.50	5.00	5.50	0.0	7.00	Volt
AUX +V	11.40	12.00	12.60	0.0	15.00	Volt
AUX -V	-11.40	-12.00	-12.60	0.0	-15.0	Volt

Figure 2-22. 73C04 Electrical Specifications

PARAMETER	MIN	TYP	MAX	UNITS
VCC Supply Current		57	75	mA
AUX +V Supply Current		76	120	mA
AUX -V Supply Current		72	120	mA

Unused drivers may be removed to reduce AUX V power consumption

Figure 2-23. Electrical Characteristics Over Recommended Operating Limits

PARAMETER	MIN	TYP	MAX	UNITS
RS-232-C Output Rate of Change			30	V/μsec
RS-232-C Baud Rate			19200	Baud

Figure 2-24. 73C04 Switching Characteristics Over Recommended Operating Limits

PARAMETER[2]	MIN	TYP	MAX	UNITS
High-Level Output Voltage[1]	8.0	10.0		Volt
Low-Level Output Voltage[1]	-8.0	-10.0		Volt
High-Level Short-Circuit Current	+6.0	+10.0	+12.0	mA
Low-Level Short-Circuit Current	-6.0	-10.0	-12.0	mA
High-Level Input Threshold Voltage	3.0			Volt
Low-Level Input Threshold Voltage	-3.0			Volt

[1] At termination resistance of 3.0K minimum
[2] Over recommended operating limits

Figure 2-25. 73C04 RS-232-C User Interface Electrical Characteristics

PIN NUMBER	OUTPUT (CMOS DRIVE)	INPUT (CMOS LOADS)		MNEMONIC	PIN NUMBER	OUTPUT (CMOS DRIVE)	INPUT (CMOS LOADS)		MNEMONIC
1			IN	+5 VOLTS	2	IN			+5 VOLTS
3			IN	GROUND	4	IN			GROUND
5				-5V	6				-5V
7	20	1		D3	8	20	1		D7
9	20	1		D2	10	20	1		D6
11	20	1		D1	12	20	1		D5
13	20	1		D0	14	20	1		D4
15		1		A7	16				A15
17		1		A6	18				A14
19		1		A5	20				A13
21		1		A4	22				A12
23		1		A3	24				A11
25		1		A2	26				A10
27		1		A1	28				A9
29		1		A0	30				A8
31		1		WR*	32		1		RD*
33		1		IORQ*	34				MEMRQ*
35		1		IOEXP	36				MEMEX
37				REFRESH*	38				MCSYNC*
39				STATUS 1*	40				STATUS 0*
41				BUSAK*	42				BUSRQ*
43				INTAK*	44		[1]		INTRQ*
45				WAITRQ*	46				NMIRQ*
47		1		SYSRESET*	48				PBRESET*
49				CLOCK*	50				CNTRL*
51	OUT			PCO	52			IN	PC
53				AUX GND	54				AUX GND
55			IN	AUX +12V	56				AUX +12V

* Low-level active logic
[1] Designates load = 10pF at 0.23 mA
CMOS load = 10pF at ±5μA

Figure 2-26. 73C04 STD Connector

SECTION 3
Operation and Programming

INTRODUCTION

The 73C04 is a general purpose serial data communications card and operates with the CMOS STD BUS card rack system. Use the 73C04 for interface to terminals, modems, printers, or other similar units.

This section describes the operation and programming of the 73C04 and includes an overview of its circuitry.

PRODUCT NOTICE

To guarantee the proper operation of the 73C04 CMOS dual UART card, care must be taken to ensure that the LOGIC GND and AUX GND are connected at the user's power supply. Pro-Log power supplies are shipped with both GNDs bused together and therefore meet these requirements. If a source other than Pro-Log is used for power supplies, care must be taken to ensure that these requirements are met.

INITIALIZATION

The 73C04 must be initialized after power-on or pushbutton reset and is then ready to send or receive serial data. The 73C04 has two independent communication channels. An Initialize Flowchart and Subroutine are shown in figures 4-4, 4-5, and 4-6, section 4 of this manual.

Since the characteristics of the industry standard 82C51A UART are unaltered for asynchronous operation in the 73C04, only a short description of its operation is included. For a detailed description of operation, consult one of the major 8251A integrated circuit suppliers, such as INTEL or NEC.

82C51A OPERATION AND PROGRAMMING

Reset the 82C51A by power-on or pushbutton reset. The UART will wait to be initialized by the CPU. Note that during this time, the UART may neither transmit nor receive data. When power is first applied, the 82C51A may come up in the Mode, Sync character, or Command format. To guarantee that the device is in the command instruction format before the reset command is issued, execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with C/$\overline{D}$ = 1 configures sync operation and writes two dummy 00H sync characters. An internal reset command (40H) may then be issued to return the device to the "idle" state.

The initialization of the 73C04, and all interfacing to the CPU is done through I/O ports. A table of these ports is shown in figure 3-1.

73C04 Port Assignments

73C04 Input Port Number Standard Mapping Function				73C04 Output Port Number Standard Mapping Function			
Don't Care	E0	0	0	E0	Baud Rate Register
Input Data Channel B	E1	1	1	E1	Output Data Channel B
Status Channel B	E2	2	2	E2	Command/Control Channel B
Input Data Channel A	E3	3	3	E3	Output Data Channel A
Status Channel A	E4	4	4	E4	Command/Control Channel A
Don't Care	E5	5	5	E5	Don't Care
Don't Care	E6	6	6	E6	Don't Care
Don't Care	E7	7	7	E7	Don't Care

Figure 3-1. 73C04 Port Address Mapping

CONTROL BYTE

As part of the initialization, two bytes are sent to the command/control port (see figure 3-1). The first byte sent is interpreted as a control byte. The control byte format is shown in figure 3-2.

Bits 0 and 1 must be set to the proper baud rate factor. The only usable baud rate factors on the 73C04 card are 16X and 64X. The rate factor causes asynchronous serial data to be transmitted or received on every 16th or 64th clock pulse. Most applications will be best suited to the 16X rate factor, since the 64X rate factor is generally too slow. Figure 3-3 lists the baud rates for each rate factor.

Bits 2 and 3 determine the number of data bits present in each data character.

Bits 4 and 5 determine the parity bit status. Select even, odd, or no parity. When even or odd parity is selected, the UART automatically inserts the correct polarity on transmit, and checks for correct polarity on receive.

Bits 6 and 7 determine the number of stop bits that will be appended to each serial byte when transmitting, and the number of stop bits allowed when receiving each serial byte.

Baud No.	Baud Rate As Shipped	Baud Rate Option 1[2]	Baud Rate Option 2[2]
16X Baud Rate Factor[1]			
0	110	75	2400
1	150	0	600
2	300	0	200
3	1200	0	75
4	1800	50	50
5	2400	0	134.5
6	4800	19200	0
7	9600	19200	0
64X Baud Rate Factor[1]			
0	27.5	18.75	600
1	37.5	0	150
2	75	0	50
3	300	0	18.75
4	450	12.5	12.5
5	600	0	33.63
6	1200	4800	0
7	2400	4800	0

[1] The 16X or 64X baud rate factor is software-selectable and is a function of the control byte

[2] Baud Rate Options 1 and 2 are jumper-selected and are explained under the "Baud Rate Range Jumpers" heading in section 2 of this manual

Figure 3-3. 73C04 Baud Rate Options

D7	D6	D5	D4	D3	D2	D1	D0
STOP BIT		PARITY	PARITY ENABLE	BITS/CHARACTER		RATE FACTOR	
00 Invalid 01 1 Stop Bit 10 1½ Stop Bits 11 2 Stop Bits		0 Odd Parity 1 Even Parity	0 Parity Disable 1 Parity Enable	00 5 Bits per Character 01 6 Bits per Character 10 7 Bits per Character 11 8 Bits per Character		00 Invalid 01 Invalid 10 Async Mode 16X Baud Rate 11 Async Mode 64X Baud Rate	

Figure 3-2. 73C04 Control Byte Format

COMMAND BYTE

After reset, the second byte and every subsequent byte sent to the command/control port is interpreted as a command byte. The command byte may, therefore, be sent at any time to modify UART operation. The format of the command word is shown in figure 3-4.

Bit 0 of the command word is the transmit enable bit. Data cannot be output from the UART unless this bit is in the active state.

Bit 1 of the command word is the equipment ready output bit. When the 73C04 channel is configured as DTE, it sets the data terminal ready (DTR) signal. When the 73C04 channel is configured as DCE, it sets the data set ready (DSR) signal. This bit and the transmit handshake bit control outgoing handshaking.

Bit 2 is the receive enable command bit. This bit enables the received ready flag of the status port. However, this bit does not prevent the assembly of serial characters.

Bit 3 is the send break command bit. When this bit is set, the serial transmitted data is interrupted and a continuous low level (spacing) signal is transmitted. This signal will continue as long as this bit is set.

Bit 4 is the error reset bit. It clears the three error flags of the status port. This bit performs a momentary function.

Bit 5 is the transmit handshake bit. When the 73C04 is configured as DTE, this bit sets the request to send (RTS) signal. When the 73C04 is configured as DCE, it sets the clear to send (CTS) signal. This bit and the Equipment Ready Output bit control outgoing handshaking.

Bit 6 is the software reset bit performing a momentary function. The UART channel enters the reset state (see the beginning of this section).

Bit 7 is not used and should be 0.

D7	D6	D5	D4	D3	D2	D1	D0
—	SR	TH	ER	SBRK	REN	ERO	TEN
(Not Used)	Software Reset	Transmit Handshake	Error Flag Flag Reset	Send Break	Receive Enable	Equipment Ready Output	Transmit Enable
0	0 Inactive 1 Momentary Active	0 Inactive 1 Active (RTS for DTE, CTS for DCE)	0 Inactive 1 Momentary Active	0 Inactive 1 Active	0 Inactive 1 Active	0 Inactive 1 Active (DTR (DTR for DTE, DSR for DCE)	0 Inactive 1 Active

Figure 3-4. 73C04 Command Byte Format

STATUS BYTE

The status byte for each channel always contains the present status of that channel, and can be read by the processor at any time. The status byte for each channel may be obtained by reading the port address shown in figure 3-1. The format of the status byte is shown in figure 3-5.

Bit 0 is the transmit ready bit. It indicates that the transmit character buffer is empty and that the UART can accept a new character for transmission. This bit is cleared when the transmit buffer is loaded by the CPU. Bit 0 should be used to determine when to output the next data byte.

Bit 1 is the receive ready bit, which indicates that the receive buffer has a character available. This bit is cleared when the receive buffer has been emptied by the CPU.

Bit 2 indicates when the transmit output buffer is empty.

Bit 3 is the parity error signal which indicates that the received character has a parity error. This bit is reset by the error reset bit in the command word.

Bit 4 is the overrun error bit which indicates that the received character has been overwritten by the next character. This bit is reset by the error reset bit in the command word.

Bit 5 is the framing error bit which indicates that the received character has an incorrect number of bits or the wrong number of stop bits. This bit is reset by the error reset bit in the command word.

Bit 6 is the break detect bit. This bit goes high when the receiver remains low through two consecutive stop bit sequences, indicating a break in transmission.

Bit 7 is the equipment ready input bit which indicates the status of the incoming handshake line. When the 73C04 channel is configured as DTE, this bit indicates the state of data set ready (DSR) line. When the 73C04 channel is configured as DCE, it indicates the state of the data terminal ready (DTR) line.

D7	D6	D5	D4	D3	D2	D1	D0
ERI	BRK DET	FE	OE	PE	IOE	RRDY	TRDY
Equipment Ready Input	Break Detect	Framing Error	Overrun Error	Parity Error	Transmit Output Buffer Empty	Receive Ready Bit	Transmit Ready Bit
0 Inactive 1 Active (DRS or DTE. DTR for DCE)	0 Inactive 1 Active	0 Inactive 1 Active	0 Inactive 1 Active	0 Inactive 1 Active	0 Inactive 1 Active	0 Inactive 1 Active	0 Inactive 1 Active

Figure 3-5. 73C04 Status Byte Format

BAUD RATE RANGE

The onboard baud rate circuits provide the UART with eight software-selectable baud rates. The 73C04 card is shipped with one set of baud rates already selected. There also are two optional sets of baud rates available to the user. To alter baud rates, you must change specific on-card jumpers. The proper jumper arrangement for each of the baud rate options is explained in section 2 under the "Baud Rate Range Jumpers" heading.

BAUD RATE SELECTION

The on-card baud rate jumpers select a set of eight baud rates. Each of the eight baud rates are available to both UARTs. Before transmitting or receiving, select which of the eight baud rates each UART will use. This selection is done with the baud rate register. The format of the baud rate register is shown in figure 3-6 and the baud rates are shown in figure 3-3. Notice that the baud rate is also affected by the rate factor. See control byte explanation for details. The port address for the baud rate register is shown in figure 3-1.

D7	D6	D5	D4	D3	D2	D1	D0
EA	Baud Rate A			EB	Baud Rate B		
Interrupt Enable channel A	Selects channel A baud rate			Interrupt Enable channel B	Selects channel B baud rate		
0= Disable polled interrupt 1= Enable polled interrupt	Use "Baud No." shown in figure 3-3			0= Disable polled interrupt 1= Enable polled interrupt	Use "Baud No." shown in figure 3-3		

Figure 3-6.73C04 Baud Rate Register Format

INTERRUPT OPERATION

There are two 82C51A UART chips on the 73C04. Each 82C51A has one Receive Ready line and one Transmit Ready line. The Transmit Ready line in the active state signifies the transmit buffer in the 82C51A is empty and can be given a character to transmit. The Receive Ready line in the active state signifies the receive buffer has received a character and is ready for the CPU to read that character. These four ready lines are the four interrupt lines that are brought out to connector J2 on the 73C04 (see figure 2-18). The polled interrupt logic on the 73C04 must be disabled to incorporate a priority interrupt scheme. This is done by clearing bits 7 and 3 of the baud rate register (see figure 3-6).

If the individual interrupts on connector J2 do not fit your application, the 73C04 can be used in the polled interrupt mode. When the 73C04 is in the polled interrupt mode, all four of its ready lines are wire-ORed together onto the STD BUS INTRQ* line (pin 44). In this mode the CPU must poll each interrupting device in the system to determine if that device needs service. When the 73C04 is used in the polled interrupt mode, both channel A and channel B interrupts can be software enabled or disabled (see figure 3-6). When they are enabled, the 73C04 can send an interrupt request to the CPU each time service is required.

The interrupts are acknowledged (cleared) when the CPU takes action on the request. This includes reading a data byte when the RRDY bit is asserted or writing a data byte when the TRDY bit is asserted. The 73C04's interrupts continue to be enabled.

SOFTWARE POLLING OPERATION WITHOUT INTERRUPT

The 73C04 may be used without the interrupting capability by clearing bits 7 and 3 of the baud rate register (see figure 3-6). With these bits cleared, the 73C04 will not interrupt the CPU. The CPU can, at any time, input present status from the 82C51A chips. There is one status port address for channel A and one status port address for channel B (see figure 3-1).

OVERVIEW OF OPERATING CIRCUITS

Card Select Decoder

U2 and U3 are the card select decoders. They decode IOEXP and A3 through A7. The outputs of U2 and U3 go to SX and SY. SX and SY are used to select which addresses will enable the 73C04 card. Figure 3-7 shows the card select decoder.

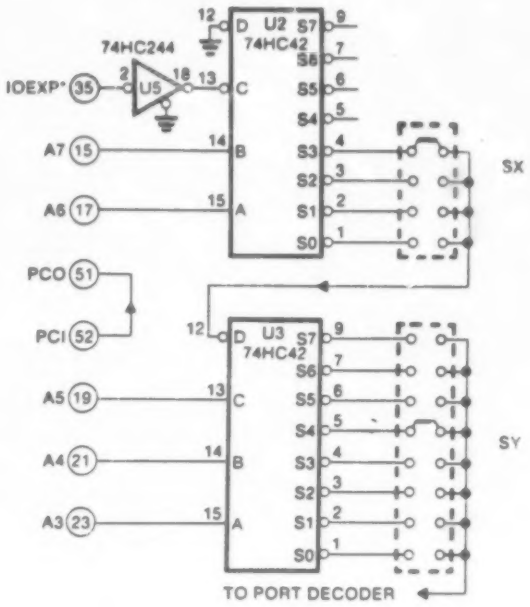


Figure 3-7. 73C04 Card Select Decoder

ol Line Logic

e control lines are all buffered by U5 which is a 24[illegible] The buffered SYSRESET* signal (RST*) is ed by U16. This provides both polarities of reset e 73C04 card. The inverted RST* (RST) is used to . th[illegible] UARTs. U6 (Gate 1) ANDs card select* and Q* [illegible] form the data bus enable signal EN*. U6 (Gate NDs RD* and IORQ* to form IORD*. U6 (Gate 3) Os WR* and IORQ* to form IOWR*. Figure 3-8 shows co[illegible]rol line logic.

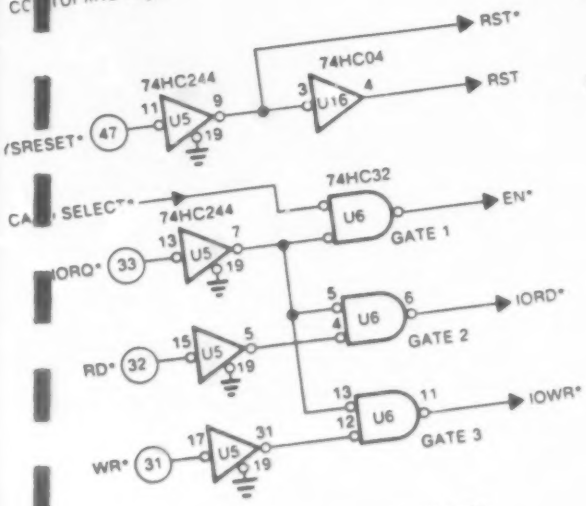


Figure 3-8. 73C04 Control Line Logic

Port Select Decoder

U4, U5, and U6 select all of the ports on the 73C04 card. U4 decodes card select* and A0 through A2. The port select outputs of U4 drive U6 and U7. AND gate U6 (see figure 3-9) ANDs port 0 select and IOWR* to form the write strobe for the baud rate register. The lower U7 in figure 3-9 ORs together port select outputs 1 and 2 of U4. This forms the UART B chip select. The port select 1 output from U4 also goes to UART B's C/D* input. The port select 3 output from U4 also goes to UART A's C/D* input. The C/D* signal informs the UART that either its control or its data ports are being accessed.

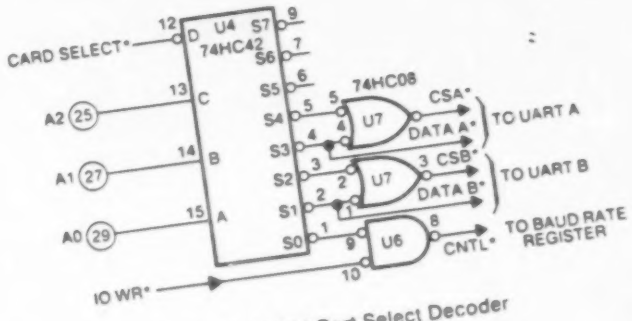


Figure 3-9. 73C04 Port Select Decoder

Data Bus Buffer and Baud Rate Register

U1 is the data bus buffer. It is enabled by the EN* signal from the control line logic circuits. The direction is controlled by the IORD* signal. U9 is the baud rate register. Data from the data bus is latched into the baud rate register (first port on this card) each time the CNTRL* line (port 0 output strobe) goes high. Output data bits 0 through 3 from U9 go to channel B. Output data bits 4 through 7 go to channel A. Figure 3-10 shows the data bus buffer and baud rate register.

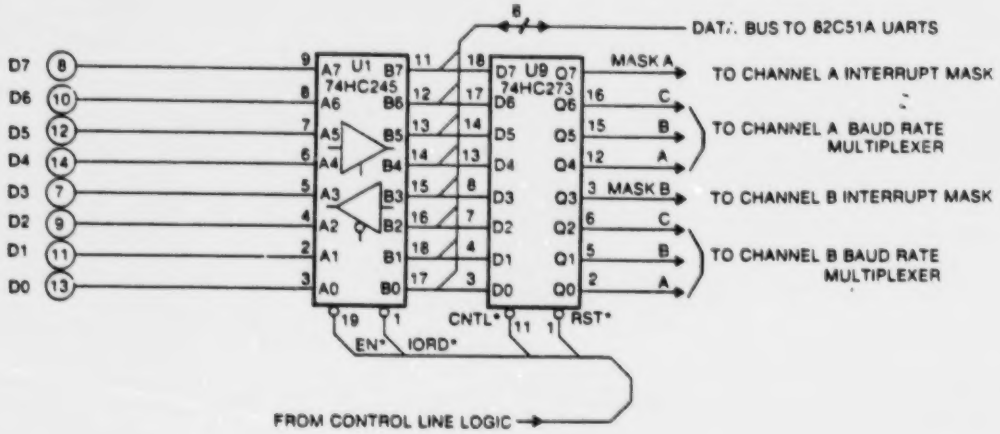


Figure 3-10. 73C04 Data Bus Buffer and Baud Rate Register

Baud Rate Generator

Figure 3-11 shows the baud rate generator. U11 and Y1 form the clock oscillator for the 73C04. The CO output of U11 is the main clock output and has a frequency of 2.4576 MHz. The Q0, Q1, and Q2 outputs count from 0 to 7. These outputs are internally connected to a divide-by-8 circuit. The output frequency (CO) drives this divider circuit. This causes Q0, Q1 and Q2 to count from 0 to 7 every eight clock cycles. Inside U11 are all the necessary divider circuits to form all the baud rates. There are always 14 baud rates generated. Inputs S0, S1, S2, and S3 are used to connect Z, the output pin, to the proper baud rate flip-flop of U11. By connecting the Q outputs to the S inputs different baud rates are generated at the Z output for every clock cycle.

The Z output is eight different baud rates multiplexed into one wire. To use one baud rate we must demulitplex this signal. U15 is the demultiplexer chip, which has eight latches addressed by Q0 to Q2 and clocked by CO. For each count of the S0 to S2 (Q0 to Q2) lines, the D inputs to a different latch. Since the Z output signal is connected to the D input, U15 is now able to latch just one of the baud rates into each of its latches. The eight outputs of U15 always output the eight baud rates.

U13 and U14, the rate multiplexers, select one of the baud rates and send it to the correct UART. U13 and U14 use the A, B, and C inputs from the baud rate register to determine which baud rate gets to the UART. Note that the frequency of the baud rates is either 16 or 64 times faster than the actual baud rate output of the UARTs.

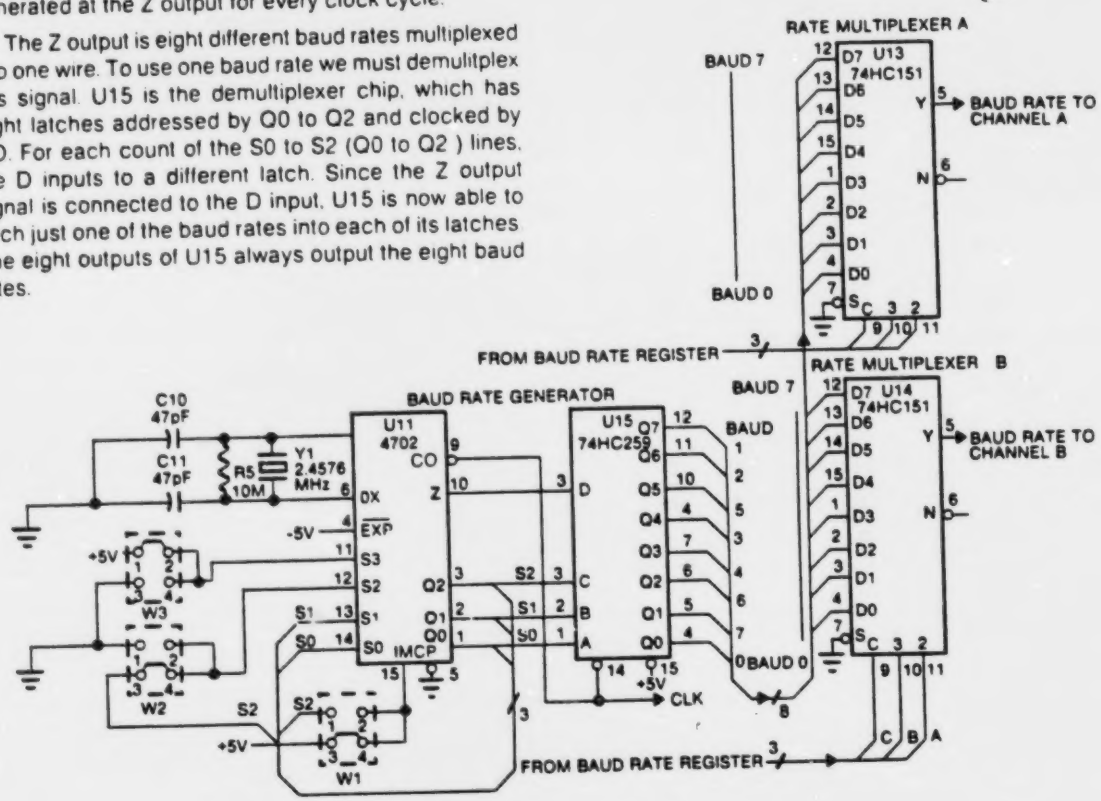


Figure 3-11. 73C04 Baud Rate Generator

Baud Rate Options

The 4702 (U11) clock generator provides more than eight baud rates; however, only eight are available at any time. To access the other frequencies, change jumpers W1, W2, and W3. Section 2 explains how to do this. Figures 3-12 through 3-14 show the signal and pin configurations, and how U11 is connected in each of the three rate options.

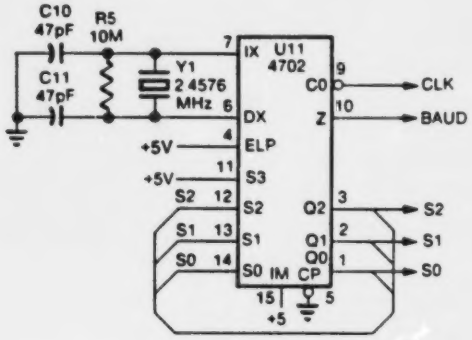


Figure 3-12. 73C04 Standard Baud Option

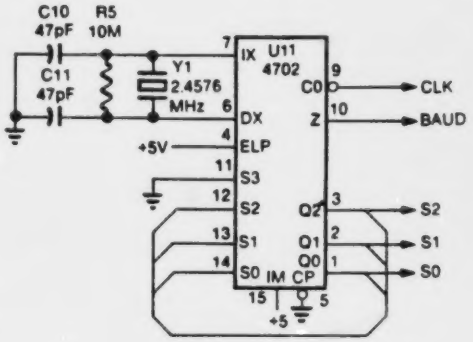


Figure 3-14. 73C04 Baud Option 2

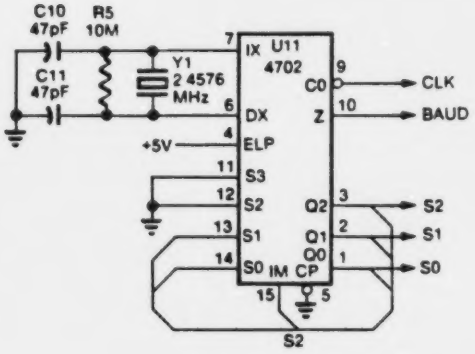


Figure 3-13. 73C04 Baud Option 1

UARTs

Figure 3-15 shows the two UARTs, U8 and U12. The internal I/O ports are enabled by CS* (pin 11). The control or data section is selected by C/D* (pin 12). The output ports are selected by WR* (pin 10). The input ports are selected by RD* (pin 13). The TXRDY signal (pin 15) goes high when the transmitter is enabled and not transmitting. The RXRDY signal (pin 14) goes high when the receiver has received a character. TD (pin 19), RTS* (pin 23), and DTR* (pin 24) are outputs. RD (pin 3), CTS* (pin 17), and DSR* (pin 22) are inputs.

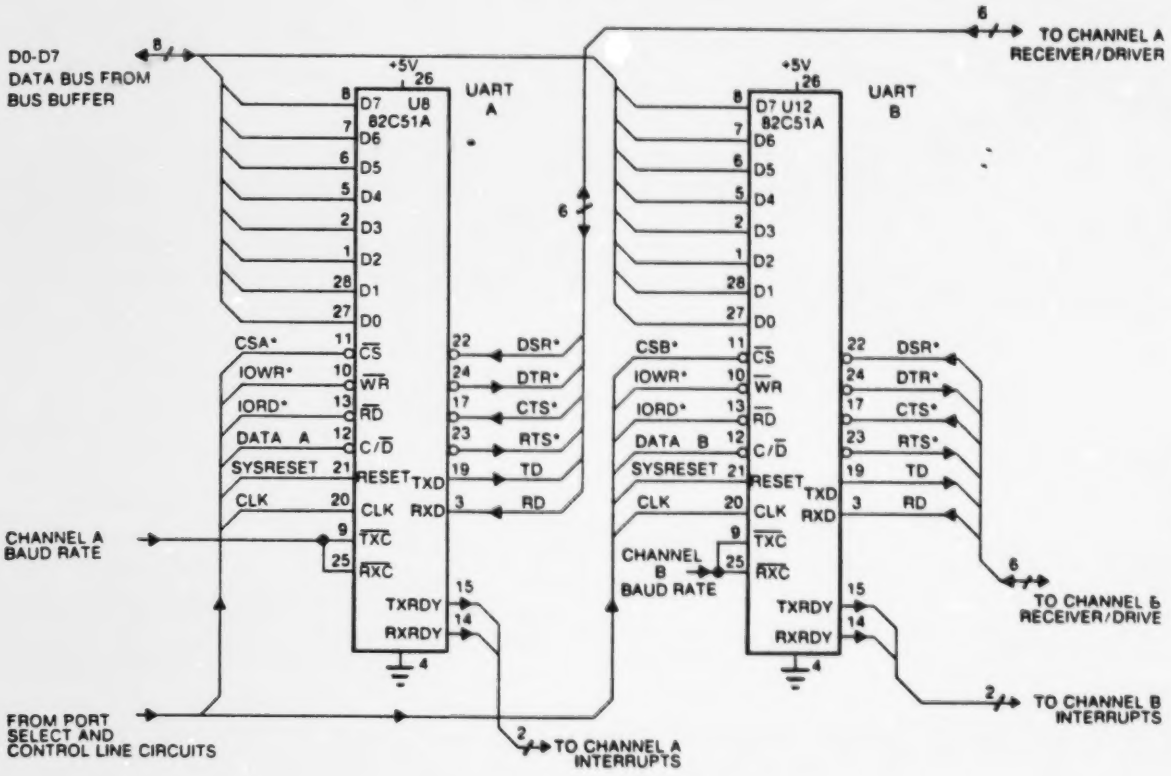


Figure 3-15. 73C04 UARTs

Interrupt Circuits

U10 is a quad open-collector NAND Gate. This gate is used to mask (disable) or unmask (enable) the polled interrupt logic on the 73C04. The ready lines from the UARTs go to these gates and are wire-ORed on the INTRQ* line (STD BUS pin 44). U16 is a hex inverter gate used to drive the interrupt connector. All four ready lines are individually sent to the interrupt connector. Figure 3-16 shows the interrupt circuits.

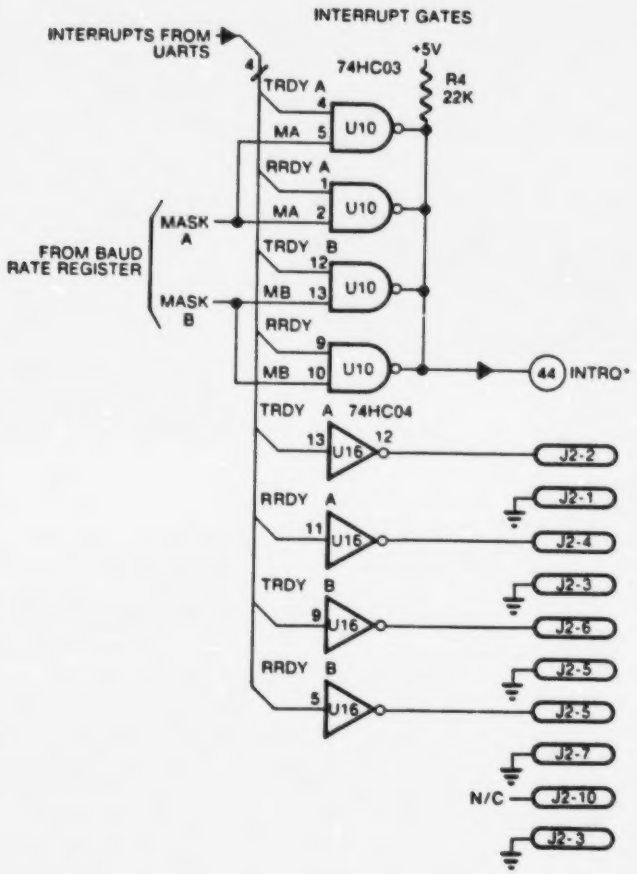


Figure 3-16. 73C04 Interrupt Circuits

RS-232-C Drivers and Receivers

U17 is the output driver chip and changes CMOS logic levels to RS-232-C logic levels. U18 is the input receiver chip and changes RS-232-C logic levels to CMOS logic levels. The mode select sockets configure the channel for either Data Terminal (DTE) or Data Communications (DCE) modes. Figure 3-17 shows U17, U18, and channel A's drivers and receivers. Channel B's RS-232-C circuit is identical.

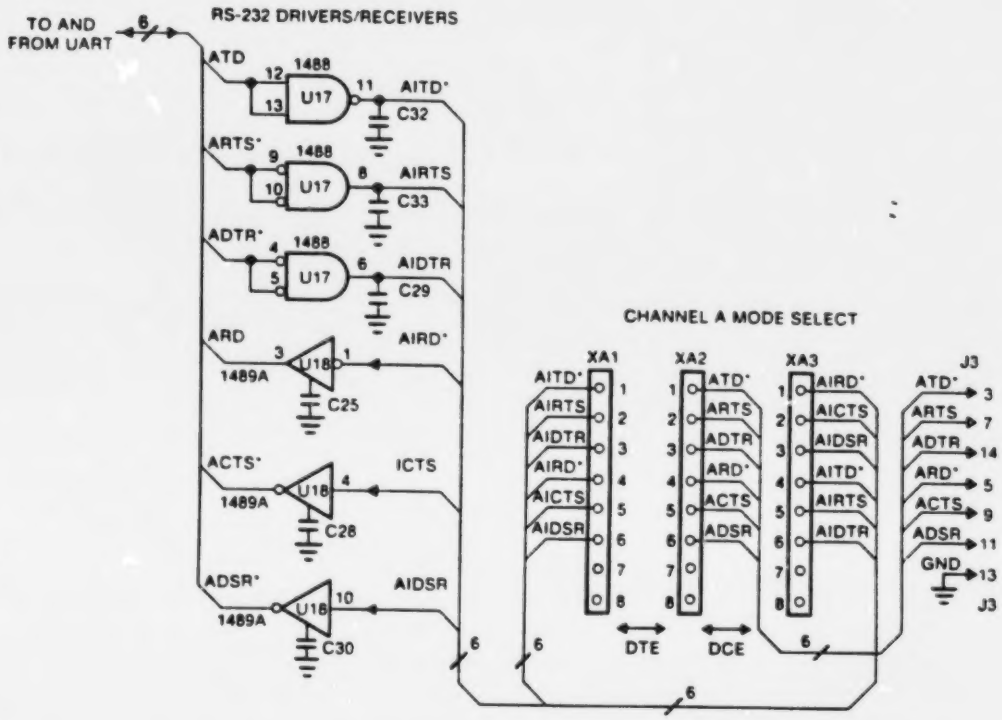


Figure 3-17. 73C04 RS-232-C Drivers and Receivers

SECTION 4
Operating Software

INTRODUCTION

This section contains hardware-level subroutine modules with which to operate the 73C04.

The software in this section can be used without license from Pro-Log. Although tested and believed correct, this software is not represented to be free from errors or copyright infringement, or appropriate for any specific application.

The subroutines are in STD instruction mnemonics, using 8080 assembly codes. They are suitable for use on 8080 code-compatible CMOS processors such as the 80C85A and CMOS Z80. The coding forms are grouped at the end of this section, following the flowcharts.

Flowcharts, which do not refer to microprocessor characteristics, allow the subroutines to be easily adapted to other microprocessor types.

The subroutines are grouped in functional modules. Each module specification describes the module's content. Individual subroutine specifications give memory, entry, and exit requirements for each path, plus timing and other necessary information.

MEMORY ADDRESSES

Full memory addresses are given. They are preferred addresses that allow the subroutines to work with those provided for other Series 7000 STD BUS cards from Pro-Log.

If your system cannot use the memory addresses in the 73C04's software package, simply change the memory page addresses, as required, when loading these modules into your system. Memory addresses that must be located in RAM are noted on the program coding forms. Other locations are intended for ROM storage, but can also be executed in RAM.

I/O PORT ADDRESSES

The 73C04's I/O ports are assigned preferred hexadecimal addresses E0-E7 for compatibility with other Series 7000 cards. Section 2 describes how to remap these addresses if necessary. This software can be used by simply changing the port addresses when loading the program modules into your system.

Note that each input (IPA) and output (OPA) instruction is extended to three bytes by the addition of a no-operation (NOP) instruction in this software. This allows the user to replace the IPA and OPA instructions with the three-byte LDAD/STAD instructions, if the 73C04 card is memory-mapped (with a memory page address decoder provided by the user on another card to generate the IORQ* signal). Also, the IPA/OPA instructions can be replaced by jump-to-ports. This allows the program to vary the port address, which in turn allows the same software package to be used for several cards in the same card rack.

SOFTWARE PACKAGE CONTENTS

Figure 4-1 lists the general purpose, hardware-level subroutines provided for operating the 73C04. These subroutines allow the user's program to communicate with the 73C04 via designated data locations in the processor's RAM. These data locations are pointed to by the HL register of the CPU.

MODULE NAME	SUBROUTINE FUNCTION	SEE FIGURE
(INITIALIZE)	This routine initializes the 73C04 card after a reset. After executing this routine the 73C04 is ready to send and receive data.	4-4, 4-5, 4-6
(WRITE UART A)	This routine will send the number in RAM out on channel A at the location pointed to by HL.	4-7, 4-8, 4-9
(WRITE UART B)	This routine will send the number in RAM out on channel B at the location pointed to by HL.	4-10, 4-11, 4-12
(READ UART A)	This routine will read one character from channel A and place it in RAM at the location pointed to by HL.	4-13, 4-14, 4-15, 4-16, 4-17
(READ UART B)	This routine will read one character from channel B and place it in RAM at the location pointed to by HL.	4-18, 4-19, 4-20, 4-21, 4-22

Figure 4-1. Index of 73C04 Subroutines

MEMORY MAPS

Figures 4-2 and 4-3 are memory maps. Figure 4-2 is a 64K memory map which shows the location of the 73C04 software package. Figure 4-3 is a page map which shows where each subroutine is located.

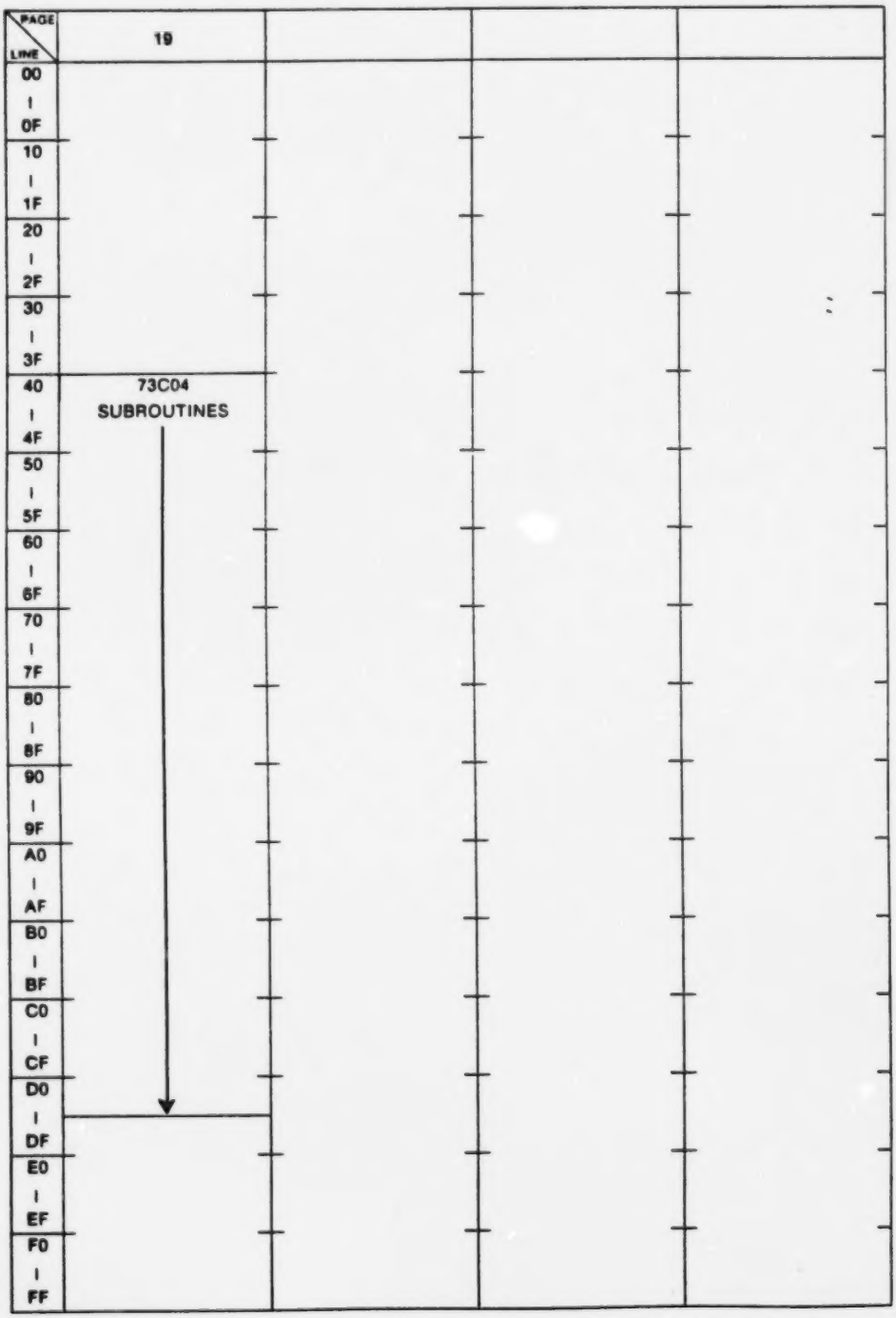


Figure 4-2. 64K Memory Map of 73C04 Subroutines

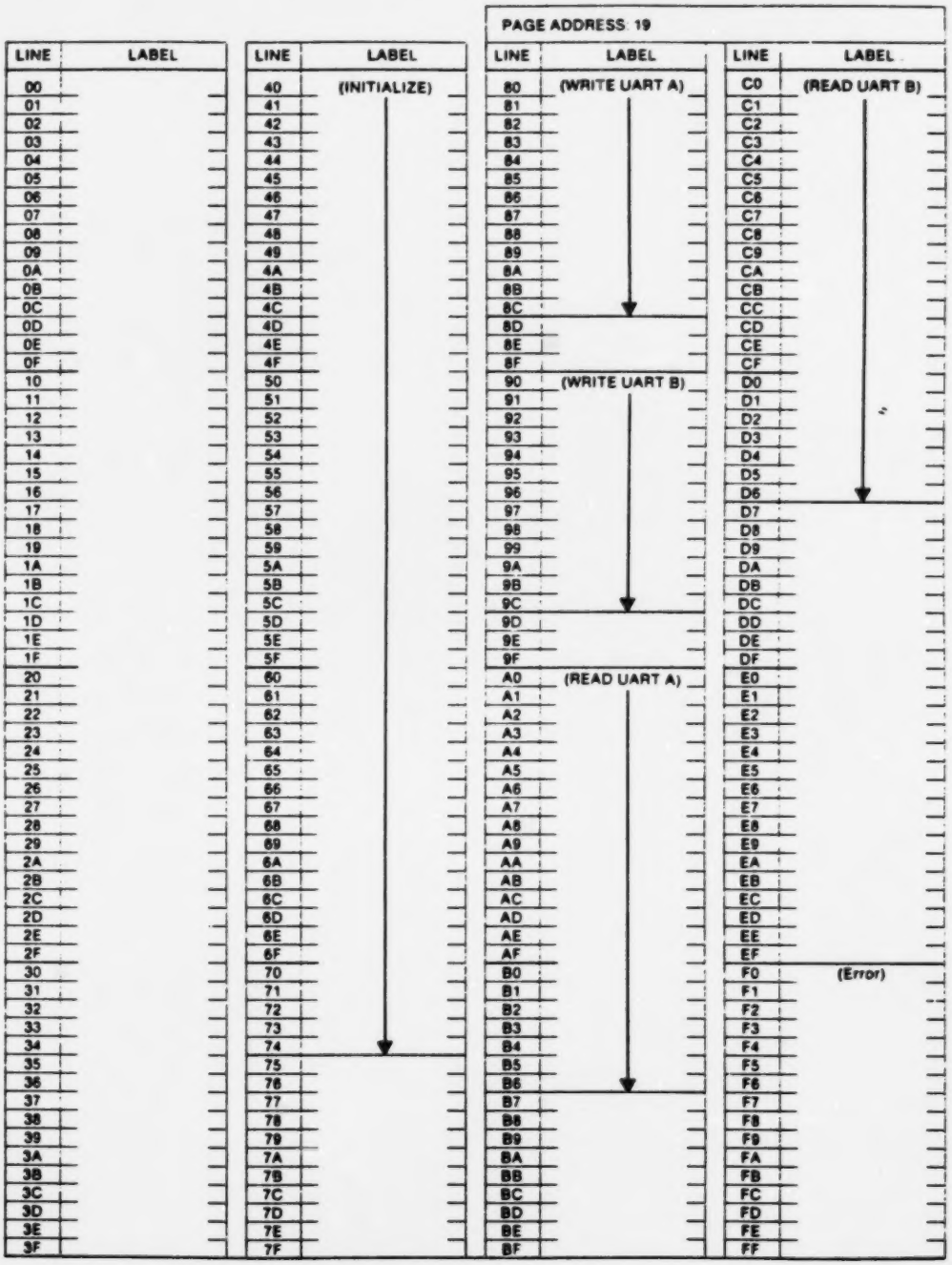


Figure 4-3. 256-Byte Memory Map of 73C04 Subroutines

(INITIALIZE) SUBROUTINE

This subroutine module initializes the 73C04 CMOS dual UART card after each power-on or pushbutton reset. Figure 4-4 is the flowchart and figures 4-5 and 4-6 present the specifications for the subroutine.

The initialize subroutine first executes the worst-case initialization sequence (see 82C51A Operation and Programming, page 3-1). The baud rates in the baud rate register are then set. Since interrupt processing is not used in these subroutines, the interrupt enable bits are set to zero. Second, the control byte is written out. Third, the command byte is written out. Since a control byte is sent, there is an assumption that the subroutine is called only once after each power on or system reset.

The UARTS are initialized with the following parameters: 9600 baud, 2 stop bits, no parity, 7 bits/character, outgoing handshake lines active, send and receive enabled. To change any of these parameters, refer to the program listings at the end of this manual.

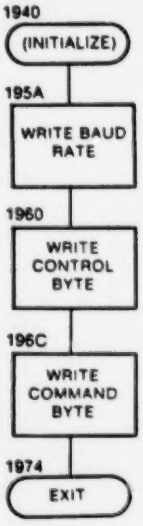


Figure 4-4. 73C04 (INITIALIZE) Flowchart

PARAMETER		ENTRY	RETURN	COMMENT
ELEMENT	ADDRESS			
Register	A	XX	Command Byte	—

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost

Figure 4-5. Register and Memory Allocation for 73C04 Subroutine (INITIALIZE)

SYMBOL	SUBROUTINE PARAMETER		LIMITS	UNITS
Ns	Stack Memory[1]		2	Bytes
Np	Program Memory		53	Bytes
Npt	Total Program Memory		53	Bytes
Nr	RAM Memory		0	Bytes
Te	Execution Time[2]	80C85A	321	Time States
		CMOS Z80	338	

NOTES:
[1] Stack Memory includes return address.
[2] Subroutine call not included in execution time.

Figure 4-6. Characteristics of 73C04 Subroutine (INITIALIZE)

(WRITE UART A) SUBROUTINE

This subroutine module takes a number from RAM, pointed to by HL, and transmits it on channel A. Figure 4-7 is the flowchart and figures 4-8 and 4-9 present the specifications for the subroutine.

The first operation performed is reading the UART status to determine if the UART transmitter is ready for a data byte. If it is, the data character is output to the data port. If the UART is not ready, the program waits until it is. After the character is output, the subroutine exits.

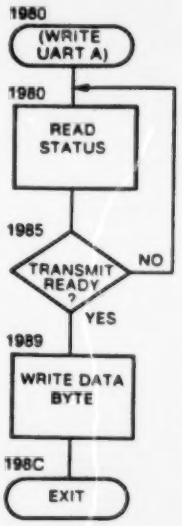


Figure 4-7. 73C04 (WRITE UART A) Flowchart

PARAMETER		ENTRY	RETURN	COMMENT
ELEMENT	ADDRESS			
Register	A	XX	Character	—
Registers	HL	Memory Address	Memory Address	—
Memory	(HL)	Character	Character	Addressed Via HL

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit
2. XX means no specific data required at entry, but entry contents will be lost.

Figure 4-8. Register and Memory Allocation for 73C04 Subroutine (WRITE UART A)

SYMBOL	SUBROUTINE PARAMETER		LIMITS	UNITS
Ns	Stack Memory[1]		2	Bytes
Np	Program Memory		13	Bytes
Npt	Total Program Memory		13	Bytes
Nr	RAM Memory[2]		1	Bytes
Te	Execution Time	80C85A	65	Min. Time States
		CMOS Z80	67	

NOTES
[1] Stack Memory includes return address
[2] May be a ROM character.

Figure 4-9. Characteristics of 73C04 Subroutine (WRITE UART A)

(WRITE UART B) SUBROUTINE

This subroutine module takes a number from RAM, pointed to by HL, and transmits it on channel B. Figure 4-10 is the flowchart and figures 4-11 and 4-12 present the specifications for the subroutine.

The first operation performed is reading the UART status to determine if the UART transmitter is ready for a data byte. If it is, the data character is output to the data port. If the UART is not ready, the program waits until it is. When the character is output, the subroutine exits.

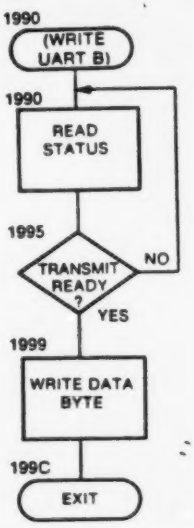


Figure 4-10. 73C04 (WRITE UART B) Flowchart

PARAMETER		ENTRY	RETURN	COMMENT
ELEMENT	ADDRESS			
Register[1]	A	XX[2]	Character	—
Registers	HL	Memory Address	Memory Address	—
Memory	(HL)	Character	Character	Addressed Via HL

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. XX means no specific data required at entry, but entry contents will be lost.

Figure 4-11. Register and Memory Allocation for 73C04 Subroutine (WRITE UART B)

SYMBOL	SUBROUTINE PARAMETER		LIMITS	UNITS
Ns	Stack Memory[1]		2	Bytes
Np	Program Memory		13	Bytes
Npt	Total Program Memory		13	Bytes
Nr	RAM Memory[2]		1	Bytes
Te	Execution Time	80C85A	65	Min. Time States
		CMOS Z80	67	

NOTES:
[1] Stack Memory includes return address.
[2] May be a ROM character.

Figure 4-12. Characteristics of 73C04 Subroutine (WRITE UART B)

(READ UART A) SUBROUTINE

This subroutine module reads a character from UART A and puts it in RAM at the location pointed to by HL. Figure 4-13 is the flowchart for the subroutine.

The first operation performed is reading the UART status to determine if the UART has received a data byte. If no character has been received, the program waits until a data byte is input. The error flags are then checked for several possible error conditions. If parity has been enabled, the parity of the character is checked against the parity bit to determine if any bits in the character were altered. An overrun error is detected if the current byte was sent while the previous byte was still in the UART. This error indicates the microprocessor system is not servicing the UART fast enough. A framing error conditions are true, the routine calls a user supplied error subroutine. If the data byte is error-free, the data byte is read, the correct number of bits are masked off, and the subroutine exits.

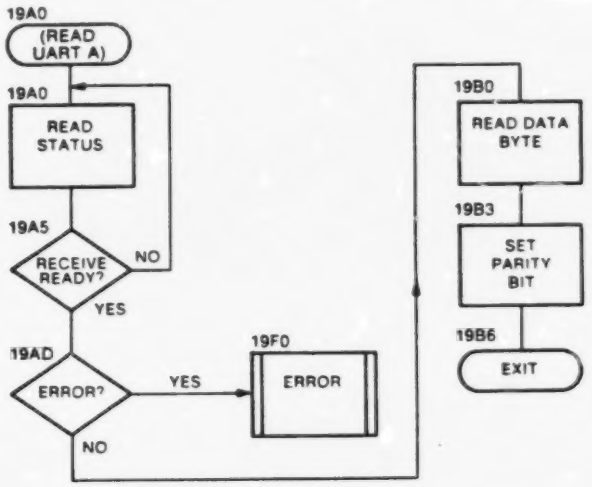


Figure 4-13. 73C04 (READ UART A) Flowchart

Figures 4-14, 4-15, 4-16, and 4-17 present specifications for the subroutine.

If the read routine exits with an error, use figures 4-14 and 4-15.

Note that when an error is encountered, this routine calls a user supplied error routine. The return address is pushed onto the stack above the original (READ UART A) subroutine return address.

PARAMETER		ENTRY	RETURN	COMMENT
ELEMENT	ADDRESS			
Register[1]	A	??[2]	Error Status	See figure 4-13

NOTES:
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. ?? means contents are unknown or meaningless.

Figure 4-14. Register and Memory Allocation for 73C04 Subroutine (READ UART A)

SYMBOL	SUBROUTINE PARAMETER		LIMITS	UNITS
Ns	Stack Memory[1,2]		4	Bytes
Np	Program Memory[1]		16	Bytes
Npt	Total Program Memory[1]		16	Bytes
Nr	RAM Memory[1]		0	Bytes
Te	Execution Time[3]	80C85A	67	Min. Time States
		CMOS Z80	58	

NOTES
[1] Stack Memory includes return address.
[2] This exit leaves with two return addresses on the stack.
[3] Does not include user supplied error routine.

Figure 4-15. Characteristics of 73C04 Subroutine (READ UART A)

If the routine exits with no errors, use figures 4-16 and 4-17.

PARAMETER		ENTRY	RETURN	COMMENT
ELEMENT	ADDRESS			
Register[1]	A	??[2]	Character	—
Registers	HL	Memory Address	Memory Address	—
RAM	(HL)	??[2]	Character	Addressed Via HL

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. ?? means contents are unknown or meaningless.

Figure 4-16. Register and Memory Allocation for 73C04 Subroutine (READ UART A)

SYMBOL	SUBROUTINE PARAMETER		LIMITS	UNITS
Ns	Stack Memory[1]		2	Bytes
Np	Program Memory		23	Bytes
Npt	Total Program Memory		23	Bytes
Nr	RAM Memory		1	Bytes
Te	Execution Time	80C85A	105	Min. Time States
		CMOS Z80	109	

NOTES
[1] Stack Memory includes return address.

Figure 4-17. Characteristics of 73C04 Subroutine (READ UART A)

(READ UART B) SUBROUTINE

This subroutine module reads a character from UART B and puts it in RAM at the location pointed to by HL. Figure 4-18 is the flowchart for the subroutine.

The first operation performed is reading the UART status to determine if the UART has received a data byte. If no character has been received, the program waits until a data byte is input. The error flags are then checked for several possible error conditions. If parity has been enabled, the parity of the character is checked against the parity bit to determine if any bits in the character were altered. An overrun error is detected if the current byte was sent while the previous byte was still in the UART. This error indicates the microprocessor system is not servicing the UART fast enough. A framing error is detected if either an incorrect number of data bits were received or if an incorrect number of stop bits were used to terminate the character. If any of these error conditions are true, the routine calls a user supplied error subroutine. If the data byte is error-free, the data byte is read, the correct number of bits are masked off, and the subroutine exits.

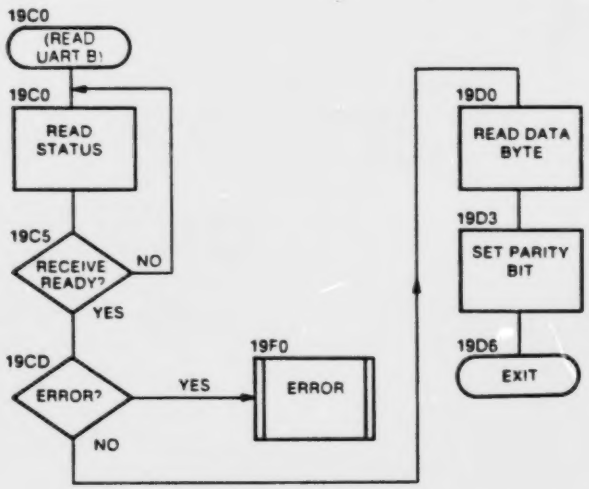


Figure 4-18. 73C04 (READ UART B) Flowchart

Figures 4-19, 4-20, 4-21, and 4-22 present specifications for the subroutines.

If the read routine exits with an error, use figures 4-19 and 4-20.

Note that when an error is encountered, this routine calls a user supplied error routine.

PARAMETER		ENTRY	RETURN	COMMENT
ELEMENT	ADDRESS			
Register[1]	A	??[2]	Error Status	See figure 4-18

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. ?? means contents are unknown or meaningless.

Figure 4-19. Register and Memory Allocation for 73C04 Subroutine (READ UART B)

SYMBOL	SUBROUTINE PARAMETER		LIMITS	UNITS
Ns	Stack Memory[1,2]		4	Bytes
Np	Program Memory[3]		53	Bytes
Npt	Total Program Memory[3]		16	Bytes
Nr	RAM Memory[3]		0	Bytes
Te	Execution Time[3]	80C85	67	Min. Time States
		CMOS Z80	68	

NOTES
[1] Stack Memory includes return address.
[2] This exit leaves with two return addresses on the stack.
[3] Does not include user supplied error routine.

Figure 4-20. Characteristics of 73C04 Subroutine (READ UART B)

If the routine exits with no errors, use figures 4-21 and 4-22.

PARAMETER		ENTRY	RETURN	COMMENT
ELEMENT	ADDRESS			
Register[1]	A	??[2]	Character	—
Registers	HL	Memory Address	Memory Address	—
Memory	(HL)	??[2]	Character	Addressed Via HL

NOTES
1. For registers not shown, entry contents are not used and remain unaltered at exit.
2. ?? means contents are unknown or meaningless.

Figure 4-21. Register and Memory Allocation for 73C04 Subroutine (READ UART B)

SYMBOL	SUBROUTINE PARAMETER		LIMITS	UNITS
Ns	Stack Memory[1]		2	Bytes
Np	Program Memory		23	Bytes
Npt	Total Program Memory		23	Bytes
Nr	RAM Memory		1	Bytes
Te	Execution Time	80C85A	105	Min. Time States
		CMOS Z80	109	

NOTE
[1] Stack Memory includes return address.

Figure 4-22. Characteristics of 73C04 Subroutine (Read UART B)

```
ADRdata!     LABEL      !INSTR !    MODIFIER    !          COMMENTS
-------!----------------!------!----------------!-----------------------------
1940 00!                !NOP   !                !
  41 00!                !NOP   !                !
  42 00!                !NOP   !                !
1943 06!(INITIALIZE)    !LDRI  !8               !INITIALIZE UARTS
  44 03!                ! ---- !03              !
  45 3E!                !LDAI  !                !
  46 00!                ! ---- !00              !
  47 D3!                !OPA   !                !
  48 E2!                ! ---- !E2              !
  49 00!                !NOP   !                !
  4A D3!                !OPA   !                !
  4B E4!                ! ---- !E4              !
  4C 00!                !NOP   !                !
  4D 05!                !DCR   !B               !
  4E C2!                !JP    !NOT ZERO        !
  4F 43!                ! ---- !(INITIALIZE)    !
1950 19!                ! ---- !                !
  51 00!                !NOP   !                !
  52 3E!                !LDAI  !                !INTERNAL RESET
  53 40!                ! ---- !40              !
  54 D3!                !OPA   !                !
  55 E2!                ! ---- !E2              !
  56 00!                !NOP   !                !
  57 D3!                !OPA   !                !
  58 E4!                ! ---- !E4              !
  59 00!                !NOP   !                !
  5A 00!                !NOP   !                !        D7 D6 D5 D4 D3 D2 D1 D0
  5B 00!                !NOP   !                !           INTERRUPT MASK B
  5C 00!                !NOP   !                !                    |
  5D 3E!                !LDAI  !                !WRITE   0  1  1  1  0  1  1  1
  5E 77!                ! ---- !77              !BAUD    |  |  |  |     |  |  |
  5F D3!                !OPA   !                !RATE    |  BAUD A     BAUD B
1960 E0!                ! ---- !E0              !        |--INTERRUPT MASK A
  61 00!                !NOP   !                !
  62 00!                !NOP   !                !
  63 3E!                !LDAI  !                !WRITE   1  1  0  0  1  0  1  0
  64 CA!                ! ---- !CA              !CONTROL STOP PARITY BITS  RATE
  65 D3!                !OPA   !                !BYTE    BITS
  66 E4!                ! ---- !E4              !
  67 00!                !NOP   !                !        * TWO STOP BITS
  68 00!                !NOP   !                !        * NO PARITY
  69 D3!                !OPA   !                !        * 7 BITS/CHARACTER
  6A E2!                ! ---- !E2              !        * 16 X RATE FACTOR
  6B 00!                !NOP   !                !
  6C 00!                !NOP   !                !
  6D 00!                !NOP   !                !  WRITE COMMAND BYTE
  6E 00!                !NOP   !                !
  6F 3E!                !LDAI  !                !  D7  0  NOT USED
1970 37!                ! ---- !37              !  D6  0  SOFTWARE RESET
  71 D3!                !OPA   !                !  D5  1  TX HANDSHAKE
  72 E4!                ! ---- !E4              !  D4  1  ERROR FLAG RESET
  73 00!                !NOP   !                !  D3  0  SEND BREAK
  74 D3!                !OPA   !                !  D2  1  RECEIVE ENABLE
  75 E2!                ! ---- !E2              !  D1  1  EQUIPT READY OUTPUT
  76 00!                !NOP   !                !
  77 C9!  ----------    !RTS   !UNCONDITIONAL   !
  78 FF!                !      !                !
  79 FF!                !      !                !
  7A FF!                !      !                !
  7B FF!                !      !                !
  7C FF!                !      !                !
  7D FF!                !      !                !
  7E FF!                !      !                !
  7F FF!                !      !                !
```

Figure 4-23. 73C04 Software Routines

```
ADRdata!     LABEL      !INSTR !    MODIFIER    !         COMMENTS
-------!---------------!------!----------------!-----------------------------
1980 DB!(WRITE UART A) !IPA   !                !  WAIT FOR READY
  81 F4!               ! ---- !E4              !
  82 00!               !NOP   !                !
  83 E6!               !ANAI  !                !
  84 01!               ! ---- !01              !
  85 CA!               !JP    !ZERO            !
  86 80!               ! ---- !(WRITE UART A)  !
  87 19!               ! ---- !                !
  88 7E!               !LDAN  !(HL)            !  WRITE CHARACTER
  89 D3!               !OPA   !                !
  8A E3!               ! ---- !E3              !
  8B 00!               !NOP   !                !
  8C C9!   ----------  !RTS   !UNCONDITIONAL   !
  8D FF!               !      !                !
  8E FF!               !      !                !
  8F FF!               !      !                !
1990 DB!(WRITE UART B) !IPA   !                !  WAIT FOR READY
  91 E2!               ! ---- !E2              !
  92 00!               !NOP   !                !
  93 E6!               !ANAI  !                !
  94 01!               ! ---- !01              !
  95 CA!               !JP    !ZERO            !
  96 90!               ! ---- !(WRITE UART B)  !
  97 19!               ! ---- !                !
  98 7E!               !LDAN  !(HL)            !  WRITE CHARACTER
  99 D3!               !OPA   !                !
  9A E1!               ! ---- !E1              !
  9B 00!               !NOP   !                !
  9C C9!   ----------  !RTS   !UNCONDITIONAL   !
  9D FF!               !      !                !
  9E FF!               !      !                !
  9F FF!               !      !                !
19A0 DB!(READ UART A)  !IPA   !                !  WAIT FOR READY
  A1 E4!               ! ---- !E4              !
  A2 00!               !NOP   !                !
  A3 E6!               !ANAI  !                !
  A4 02!               ! ---- !02              !
  A5 CA!               !JP    !ZERO            !
  A6 A0!               ! ---- !(READ UART A)   !
  A7 19!               ! ---- !                !
  A8 DB!               !IPA   !                !  CHECK FOR ERROR
  A9 E4!               ! ---- !E4              !
  AA 00!               !NOP   !                !
  AB E6!               !ANAI  !                !
  AC 38!               ! ---- !38              !
  AD C4!               !JS    !NOT ZERO        !  USER SUPPLIED ERROR ROUTINE
  AE F0!               ! ---- !(ERROR)         !
  AF 19!               ! ---- !                !
19B0 DB!               !IPA   !                !  INPUT AND STORE CHARACTER
  B1 E3!               ! ---- !E3              !
  B2 00!               !NOP   !                !
  B3 F6!               !ORAI  !                !
  B4 B0!               ! ---- !B0              !
  B5 77!               !STAN  !(HL)            !
  B6 C9!   ----------  !RTS   !UNCONDITIONAL   !
  B7 FF!               !      !                !
  B8 FF!               !      !                !
  B9 FF!               !      !                !
  BA FF!               !      !                !
  BB FF!               !      !                !
  BC FF!               !      !                !
  BD FF!               !      !                !
  BE FF!               !      !                !
  BF FF!               !      !                !
```

Figure 4-24. 73C04 Software Routines

ADRdata	LABEL	INSTR	MODIFIER	COMMENTS
19C0 DB	(READ UART B)	IPA		WAIT FOP READY
C1 E2		----	E2	
C2 00		NOP		
C3 E6		ANAI		
C4 02		----	02	
C5 CA		JP	ZERO	
C6 C0		----	(READ UART B)	
C7 19		----		
C8 DB		IPA		CHECK FOR ERROR
C9 E2		----	E2	
CA 00		NOP		
CB E6		ANAI		
CC 38		----	38	
CD C4		JS	NOT ZERO	USER SUPPLIED ERROR ROUTINE
CE F0		----	(ERROR)	
CF 19		----		
19D0 DB		IPA		INPUT AND STORE ROUTINE
D1 E1		----	E1	
D2 00		NOP		
D3 F6		ORAI		
D4 80		----	R0	
D5 77		STAN	(HL)	
D6 C9	----------	RTS	UNCONDITIONAL	
D7 FF				
D8 FF				
D9 FF				
DA FF				
DB FF				
DC FF				
DD FF				
DE FF				
DF FF				
19E0 FF				
E1 FF				
E2 FF				
E3 FF				
E4 FF				
E5 FF				
E6 FF				
E7 FF				
E8 FF				
E9 FF				
EA FF				
EB FF				
EC FF				
ED FF				
EE FF				
EF FF				
19F0 FF	(ERROR)			USER SUPPLIED ERROR ROUTINE
F1 FF				
F2 FF				
F3 FF				
F4 FF				
F5 FF				
F6 FF				
F7 FF				
F8 FF				
F9 FF				
FA FF				
FB FF				
FC FF				
FD FF				
FE FF				
FF FF				

Figure 4-25. 73C04 Software Routines

SECTION 5
Maintenance

REFERENCE DRAWINGS

The schematic (figures 5-1 and 5-2) and assembly drawing (figure 5-3) in the following pages are included in this manual FOR REFERENCE USE ONLY. They may differ in some respects from the card and documentation that the user receives from Pro-Log. The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.

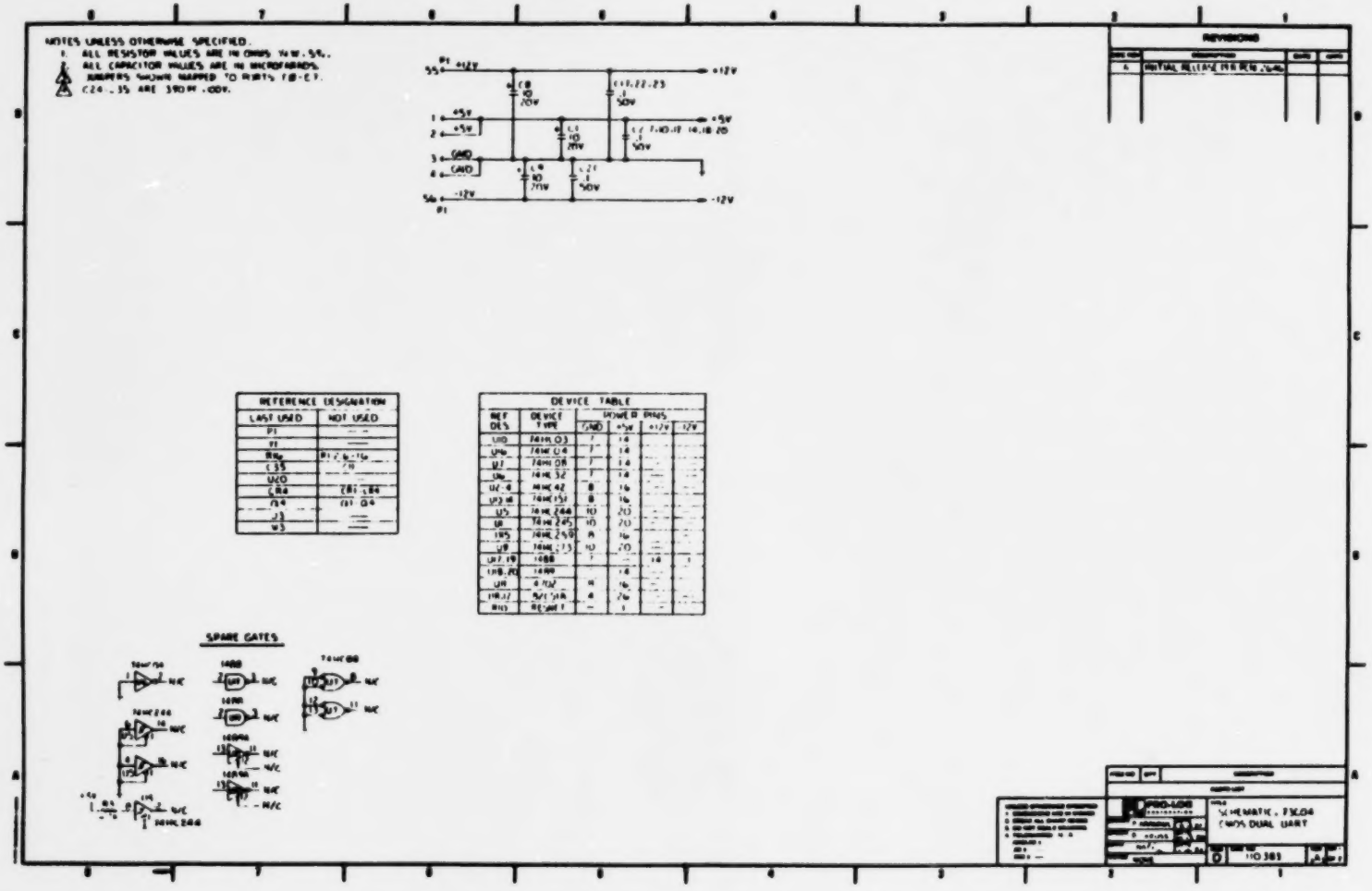


Figure 5-1. 73C04 Schematic Page 1

REFERENCE ONLY

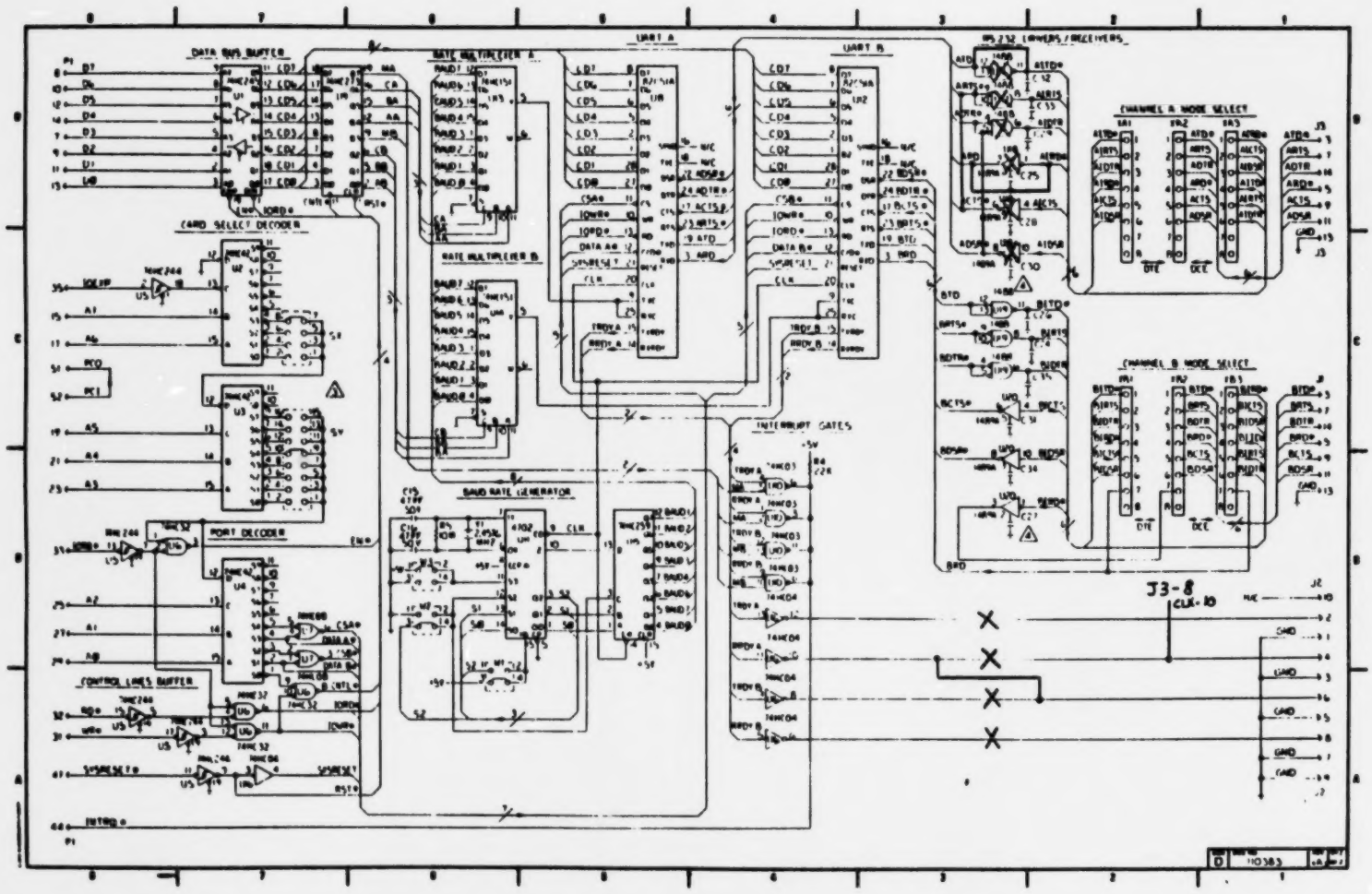


Figure 5-2. 73C04 Schematic Page 2

REFERENCE ONLY

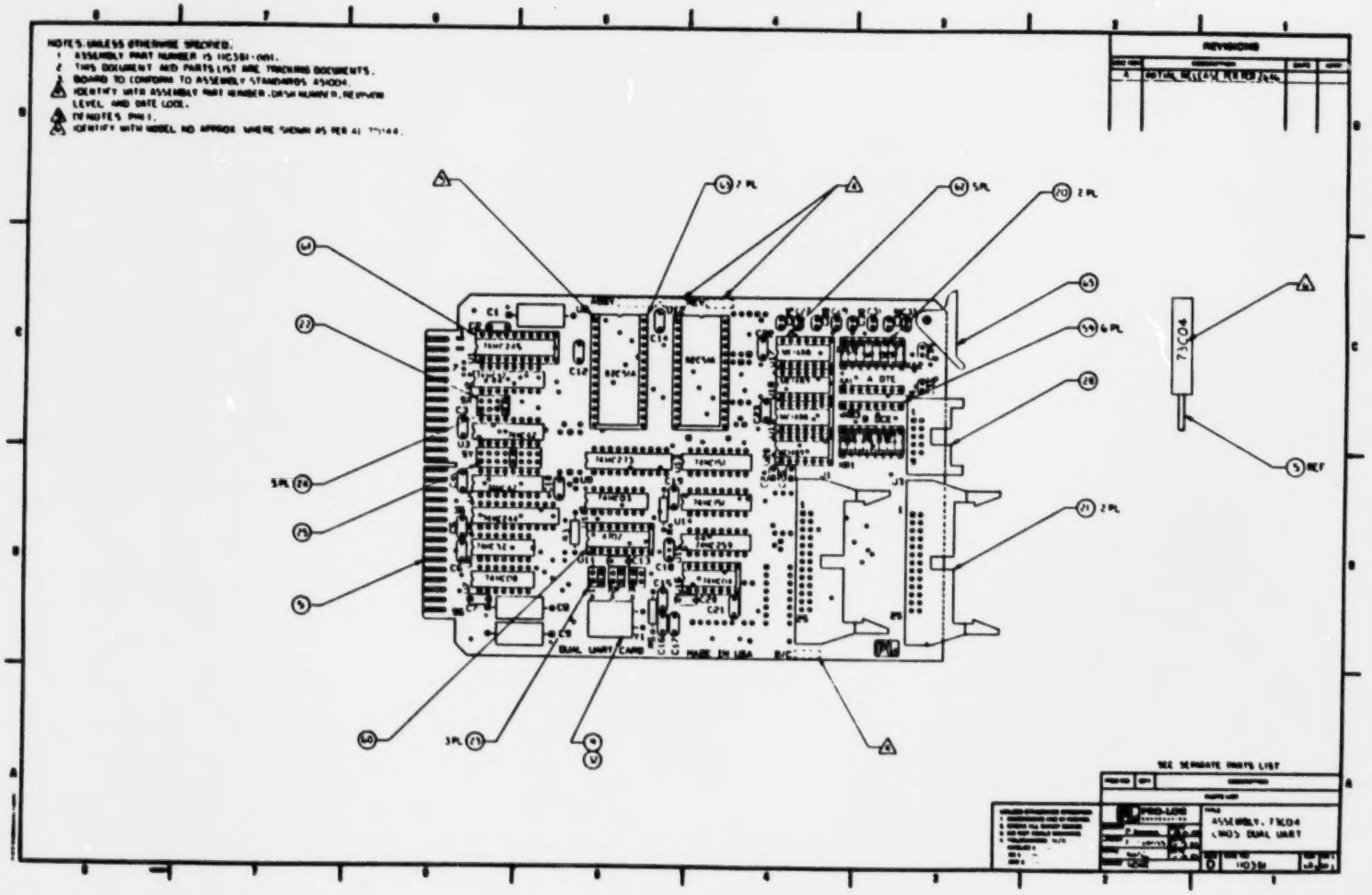


Figure 5-3. 73C04 Assembly Drawing

REFERENCE ONLY

APPENDICE H
CARTE D'ENTRÉES/SORTIES (79C04)

CRIQ

APPENDICE H.1
CARTE PRO-LOG 79C04

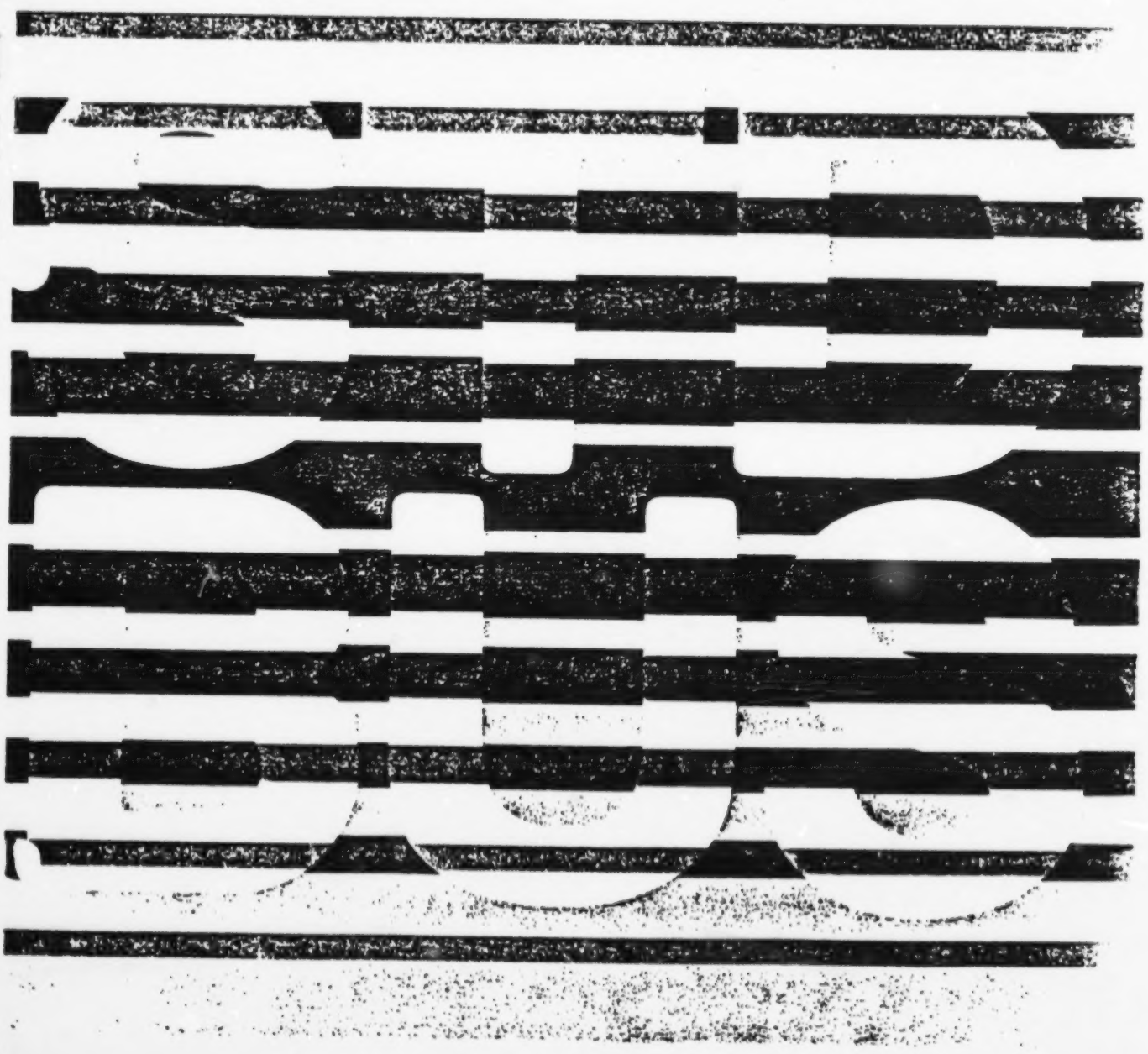
CRIQ

PRO-LOG®
CORPORATION

STD 7000

7904 TTL
79C04 CMOS
Decoded I/O Utility Card

USER'S MANUAL



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SECTION 1
Purpose and Main Features

PURPOSE

The 7904 and 79C04 are printed circuit cards designed for prototyping I/O circuitry. They provide complete STD BUS buffering and I/O port select decoding. They also provide access to the upper eight bits of the address bus, the control bus, and the power bus. A 4.0 by 4.3-inch (101.6 by 109.2 mm) grid of holes on 0.1-inch (2.54 mm) centers is provided for adding components. These plated-through holes accommodate 0.025-inch (0.64 mm) square wirewrap posts.

The 79C04 is fully implemented in CMOS to offer a high degree of noise immunity, low power consumption, and a wide temperature range.

FEATURES

- Data bus buffers with hysteresis
- Decodes 8 sequential addresses for input ports
- Decodes 8 sequential addresses for output ports
- Access to all STD BUS signals and power buses
- Plated-through holes accommodate 0.025-inch (0.64 mm) square posts
- 17.2 square inches (111 cm^2) of breadboard area
- Processor independent

ADDITIONAL FEATURES of 79C04

- High speed CMOS
- High noise immunity
- Low power consumption
- Wide temperature range

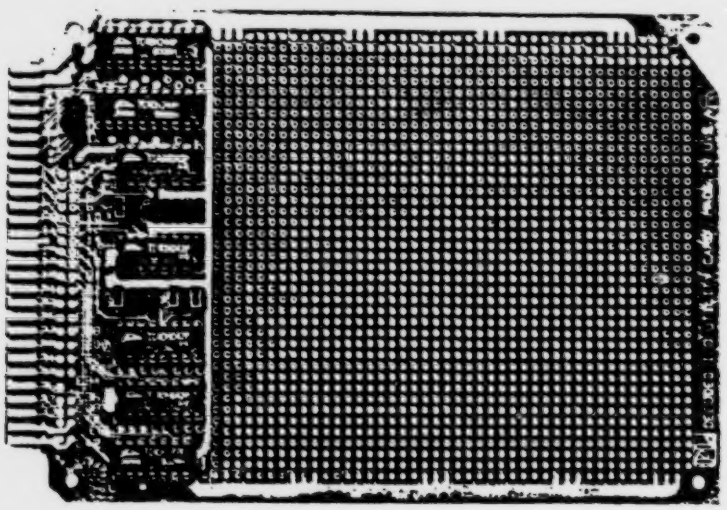


Figure 1-1. 7904/79C04 Decoder I/O Utility Card

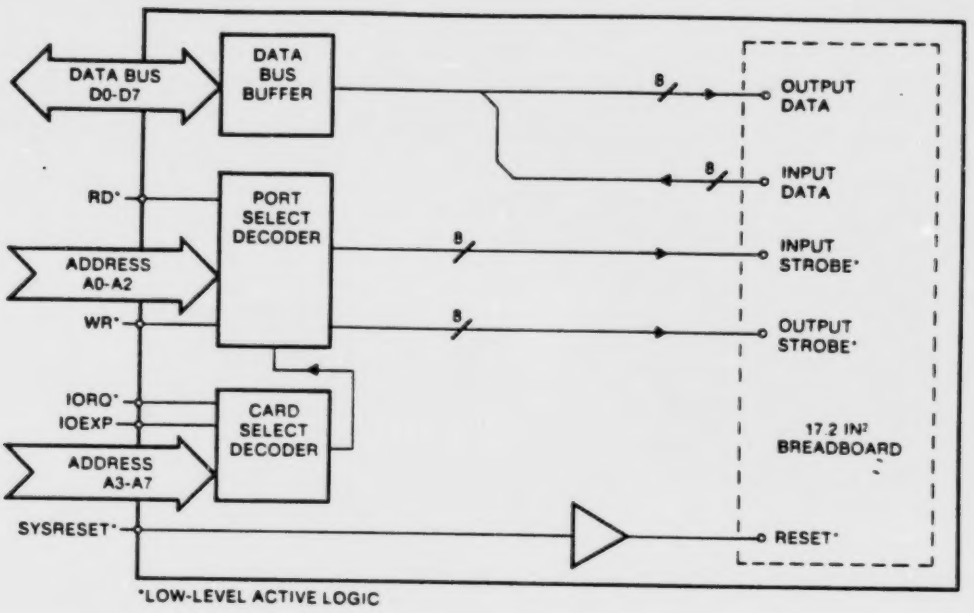


Figure 1-2. 7904/79C04 Block Diagram

FUNCTIONAL DESCRIPTION

The following describes each block in the block diagram (figure 1-2)

Data Bus Buffers — two octal buffers, one for inputs and one for outputs, provide buffering and direction control of the data bus

Card Select Decoder — two 4- to 10-line decoders decode A_3 to A_7 address lines, IORQ* and IOEXP*. A card select signal occurs when the active decoded line matches the jumper location.

Port Select Decoders — two 4- to 10-line decoders decode A_0 to A_2 address lines and RD* or WR* line to activate one of eight input port select lines (IS0-IS7), or one of eight output port select lines (OS0-OS7).

SYSRESET* Buffer — provides a means for resetting I/O latches. The signal is buffered to connect to devices in the breadboard area without overloading the STD BUS SYSRESET* line

Breadboard Area — provides a location for prototype circuits. It consists of a 4.0- by 4.3-inch grid of plated-through holes on 0.1-inch centers.

STD address and control buses are available at plated-through holes. Heavy power and ground traces along each long edge of the card are connected to plated-through holes adjacent to the breadboard area.

The breadboard area is compatible with both wire-wrapping and insulation-displacement wiring methods.

LOCATION OF SIGNIFICANT FEATURES

Figure 1-3 shows the locations of significant features of 7904 and 79C04 cards.

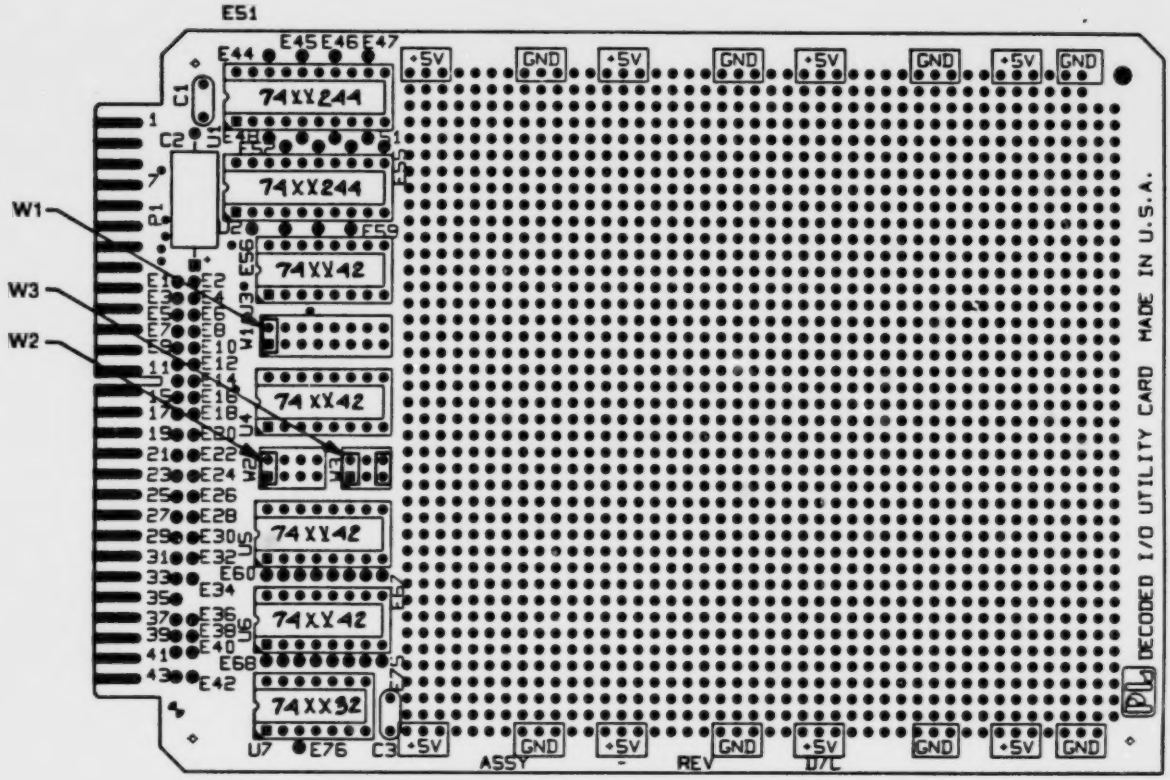


Figure 1-3. Significant Features (7904/79C04)

SECTION 2
Installation and Specifications

INSTALLATION

CAUTION

To prevent possible damage to your STD BUS system, make sure power is off before inserting a card into the card rack or removing a card from the card rack.

With the card ejector toward the top, insert the 7904 or 79C04 into any slot in the card rack. See figure 2-1. Empty slots on one or both sides of the card may be required if tall components or long wirewrap pins are used in the breadboard area.

To access the card, install it in either end of an open-ended card rack (card ejector toward the top) or use a Pro-Log 7901 card extender. Plug the 7901 into any slot in the card rack and plug the 7904 or 79C04 into the connector on the card extender.

The 79C04 is designed to operate in CMOS logic level STD systems, while the 7904 is designed for conventional LSTTL logic level systems.

CAUTION

All unconnected pins of CMOS devices must be protected from electrostatic discharge; therefore, all card connector pins must be connected together or the card enclosed in a conductive plastic bag when it is not installed in the rack.

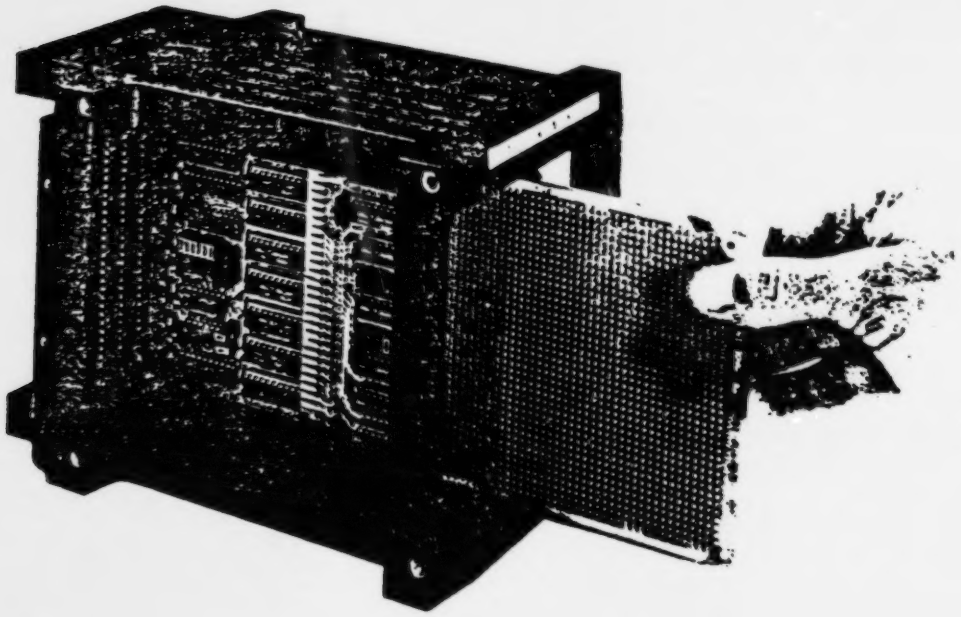


Figure 2-1. Installation (7904/79C04)

ADDRESS REMAPPING

The 7904 and 79C04 each occupy eight addresses. As shipped, they are mapped at addresses 00 to 07. The card(s) can be remapped to any eight consecutive addresses from 00 to FF by moving jumpers W1 and W2. The first of the eight addresses must be a hex number divisible by eight. Figure 2-2 (page 2-4) shows W1 and W2 jumper locations for all eight-address blocks available. Only one jumper is to be placed on each of these headers for any configuration.

TERMINATION AND LOADING

A termination network is not required for Pro-Log's CMOS STD BUS systems. (In fact, using Pro-Log's 7909A terminator card in a CMOS STD system will degrade the system performance as a result of its capacitive loading.)

Since the input impedance of CMOS is very large, the main restriction on fanout is load capacitance. As the total capacitive load on an output is increased, the propagation delays increase, along with power consumption. Since Pro-Log's 24-slot 7106 motherboard uses terminatino that presents large capacitive loads, it should not be used with CMOS cards. Check any other termination in the system for capacitive loading and power dissipation.

ALTERNATE DATA BUS BUFFER SELECTION

Header W3 provides a means for selecting the data bus buffers with alternate circuitry. See schematic, figures 5-1 and 5-2 (pages 5-2 through 5-5). The input buffer (U2) can be permanently selected by connecting its Select line to ground with a jumper between pins 4 and 6 of W3. Output buffer U1 can similarly be selected by placing a jumper between pins 1 and 3 of W3. The buffers can also be controlled by the user's logic by removing the jumpers and making wirewrap connections from the user's logic to header W3, pins 1 and 6.

ADDR	JUMPERS
00	W1: 1-2* W2: 1-2*
01	
02	
03	
04	
05	
06	
07	
08	W1: 1-2 W2: 3-4
09	
0A	
0B	
0C	
0D	
0E	
0F	
10	W1: 1-2 W2: 5-6
11	
12	
13	
14	
15	
16	
17	
18	W1: 1-2 W2: 7-8
19	
1A	
1B	
1C	
1D	
1E	
1F	
20	W1: 3-4 W2: 1-2
21	
22	
23	
24	
25	
26	
27	
28	W1: 3-4 W2: 3-4
29	
2A	
2B	
2C	
2D	
2E	
2F	
30	W1: 3-4 W2: 5-6
31	
32	
33	
34	
35	
36	
37	
38	W1: 3-4 W2: 7-8
39	
3A	
3B	
3C	
3D	
3E	
3F	

ADDR	JUMPERS
40	W1: 5-6 W2: 1-2
41	
42	
43	
44	
45	
46	
47	
48	W1: 5-6 W2: 3-4
49	
4A	
4B	
4C	
4D	
4E	
4F	
50	W1: 5-6 W1: 5-6
51	
52	
53	
54	
55	
56	
57	
58	W1: 5-6 W2: 7-8
59	
5A	
5B	
5C	
5D	
5E	
5F	
60	W1: 7-8 W2: 1-2
61	
62	
63	
64	
65	
66	
67	
68	W1: 7-8 W2: 3-4
69	
6A	
6B	
6C	
6D	
6E	
6F	
70	W1: 7-8 W2: 5-6
71	
72	
73	
74	
75	
76	
77	
78	W1: 7-8 W2: 7-8
79	
7A	
7B	
7C	
7D	
7E	
7F	

ADDR	JUMPERS
80	W1: 9-10 W2: 1-2
81	
82	
83	
84	
85	
86	
87	
88	W1: 9-10 W2: 3-4
89	
8A	
8B	
8C	
8D	
8E	
8F	
90	W1: 9-10 W1: 5-6
91	
92	
93	
94	
95	
96	
97	
98	W1: 9-10 W2: 7-8
99	
9A	
9B	
9C	
9D	
9E	
9F	
A0	W1: 11-12 W2: 1-2
A1	
A2	
A3	
A4	
A5	
A6	
A7	
A8	W1: 11-12 W2: 3-4
A9	
AA	
AB	
AC	
AD	
AE	
AF	
B0	W1: 11-12 W2: 5-6
B1	
B2	
B3	
B4	
B5	
B6	
B7	
B8	W1: 11-12 W2: 7-8
B9	
BA	
BB	
BC	
BD	
BE	
BF	

ADDR	JUMPERS
C0	W1: 13-14 W2: 1-2
C1	
C2	
C3	
C4	
C5	
C6	
C7	
C8	W1: 13-14 W2: 3-4
C9	
CA	
CB	
CC	
CD	
CE	
CF	
D0	W1: 13-14 W2: 5-6
D1	
D2	
D3	
D4	
D5	
D6	
D7	
D8	W1: 13-14 W2: 7-8
D9	
DA	
DB	
DC	
DD	
DE	
DF	
E0	W1: 15-16 W2: 1-2
E1	
E2	
E3	
E4	
E5	
E6	
E7	
E8	W1: 15-16 W2: 3-4
E9	
EA	
EB	
EC	
ED	
EE	
EF	
F0	W1: 15-16 W2: 5-6
F1	
F2	
F3	
F4	
F5	
F6	
F7	
F8	W1: 15-16 W2: 7-8
F9	
FA	
FB	
FC	
FD	
FE	
FF	

Figure 2-2. Port Address Mapping (7904/79C04)

SPECIFICATIONS

Electrical

7904

MNEM.	PARAMETER	Recommended Operating Limits			Absolute Nonoperating Limits		UNITS
		MIN	TYP	MAX	MIN	MAX	
Vcc	Supply Voltage	4.75	5.00	5.25	0	7.00	Volts

79C04

MNEM.	PARAMETER	Recommended Operating Limits[1]			Absolute Nonoperating Limits		UNITS
		MIN	TYP	MAX	MIN	MAX	
Vcc	Supply Voltage	4.50	5.00	5.50	0	7.00	Volts

[1] For TTL interfacing, supply voltage must be 5±0.25V

Figure 2-3. Electrical Specifications (7904/79C04)

Environmental

7904

PARAMETER	Recommended Operating Limits			Absolute Nonoperating Limits		UNITS
	MIN	TYP	MAX	MIN	MAX	
Free Air Temperature	0	+25	+65	-40	+75	°C
Humidity	5	—	95[1]	5	95[1]	%RH

79C04

PARAMETER	Recommended Operating Limits			Absolute Nonoperating Limits		UNITS
	MIN	TYP	MAX	MIN	MAX	
Free Air Temperature	40	+25	+85	-40	+100	°C
Humidity	5	—	95[1]	5	95[1]	%RH

[1] Noncondensing

Figure 2-4. Environmental Specifications (7904/79C04)

Supply Current

7904

MNEM.	PARAMETER	OPERATING LIMITS			UNITS
		MIN	TYP	MAX	
Icc	Vcc Supply Current	—	92	162	mA

79C04

MNEM.	PARAMETER	OPERATING LIMITS[1,2]			UNITS
		MIN	TYP	MAX	
Icc	Vcc Supply Current	—	0.02	0.2	mA

[1] Quiescent value with all inputs at Vcc or GND.
[2] Supply current for logic provided. Add user circuitry supply current.

Figure 2-5. Supply Current Over Operating Range (7904/79C04)

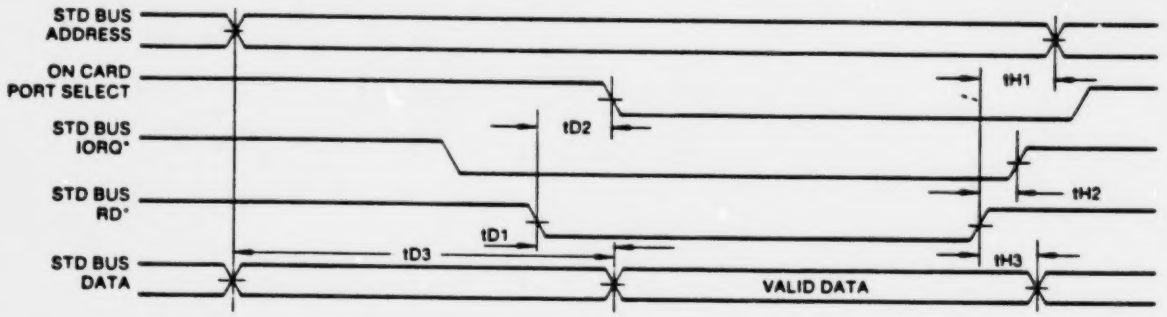
Mechanical

The 7904 and 79C04 meet all general STD mechanical specifications.

TIMING

7904 and 79C04 STD BUS timing is shown in figures 2-6 and 2-7. In each figure, the signal is shown with the implied condition that all other signals are valid before the signal becomes valid. Timing data is exclusive of circuitry added by the user. These timing diagrams are independent of CPU card timing, but must be compared with the CPU card timing to ensure that the 7904 or 79C04 decoding and your breadboarded logic can respond to the CPU in the time allowed for I/O operations.

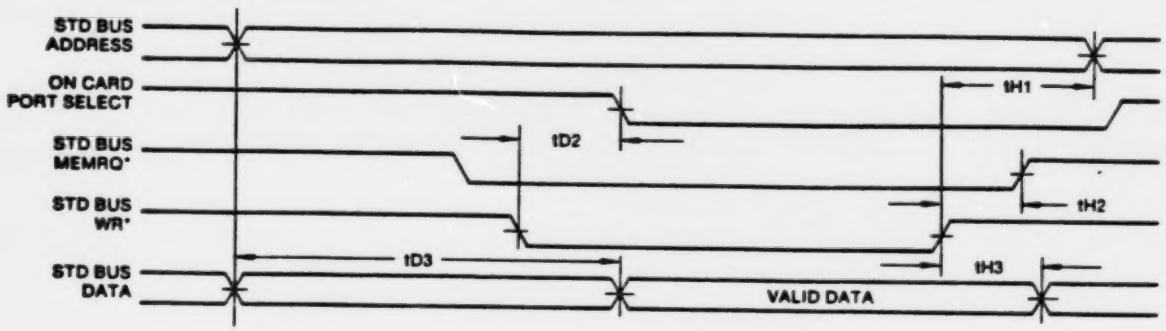
All times given are in nanoseconds. Timing given is for the entire operating supply voltage and temperature ranges.



SYMBOL	PARAMETER	7904		79C04	
		MIN	MAX	MIN	MAX
tD1	Data delay from RD* active		62		146
tD2	Port select active from RD* active		62		116
tD3	Data delay from Address		134		282
tH1	Address hold after RD* inactive	50		179	
tH2	IORQ* hold after RD* inactive	50		179	
tH3	Data hold after RD* inactive	0		150	

All times given in nanoseconds.

Figure 2-6. Input Timing



SYMBOL	PARAMETER	7904		79C04	
		MIN	MAX	MIN	MAX
tD1	Data delay from WR* active		62		146
tD2	Port select active from WR* active		62		116
tD3	Data delay from Address		134		282
tH1	Address hold after WR* inactive	50		179	
tH2	IORQ* hold after WR* inactive	50			
tH3	Data hold after WR* inactive	0		150	

All times given in nanoseconds

Figure 2-7. Output Timing

STD INTERFACE

Figures 2-8 and 2-9 show the STD pinout, loading and drive presented by the 7904 and 79C04.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)		PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5V	VCC		2	1		VCC	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX -V

* Low-level active logic

Figure 2-8. STD Edge Connector (7904)

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)		PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	20	8	7	20	1	D3
D6	1	20	10	9	20	1	D2
D5	1	20	12	11	20	1	D1
D4			14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51		OUT	PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX -V

† CMOS LOAD = pF at ±5 μA
* Low-level active logic

Figure 2-9. STD Edge Connector (79C04)

SECTION 3
Operation and Programming

INTRODUCTION

The operation of these cards can best be explained by describing a specific application. As explained earlier, each card can be used for as many as eight input and eight output ports; however, the application chosen is one using two input and two output ports.

APPLICATION EXAMPLE

Specification

The following application example shows how to design and build a card with the following functions:

- One-digit, seven-segment readout at address 25H
- One 8-bit, latched output port at address 23H
- Two 8-bit, buffered input ports at addresses 21H and 25H
- One I/O connector for connection to the input and output lines
- SYSRESET* used for clearing the output port and the readout

Refer to figure 3-1 for a block diagram of this circuit.

Port Address Mapping

Refer to figure 2-2 (page 2-3) to determine where the W1 and W2 jumpers must be placed to map the ports to the specified addresses. All specified addresses are within a block of eight. The block is 20H to 27H and the figure shows that W1 must be at 3-4 and W2 at 1-2.

Referring to the schematic in figure 5-1 (page 5-2) it is evident that, with the card mapped from 20 to 27, output port select lines OS3* (E71) and OS5* (E73) from U6 must be used for the output ports 23H and 25H, and input port select lines IS1* (E61) and IS5* (E65) from U5 must be used for input ports 21H and 25H.

The output port select lines are connected to the Clock inputs of the output latches and the input port select lines are connected to the Enable lines of the input buffers.

The four output lines from output port 25H are connected to the inputs of the BCD to the 7-segment decoder/driver, and the 7-output lines from this are in turn connected to the 7-segment display.

SYSRESET* (E76) is connected to the Clear inputs of each of the output latches. All incoming data lines (E44 through E51) are connected to the data input lines of output latch 2; the four lower ones (E44 through E47) are connected to the four input lines used on output latch 1. All outgoing data lines (E52 through E59) are connected to the eight input lines of each of the input buffers.

All the lines from output port 25H and input ports 21H and 25H are connected to the I/O connector.

The output port select lines are connected to the Clock inputs of the output latches and the input port select lines are connected to the Enable lines of the input buffers.

The four output lines from output port 25H are connected to the inputs of the BCD to the 7-segment decoder/driver, and the 7-output lines from this are in turn connected to the 7-segment display.

SYSRESET* (E76) is connected to the Clear inputs of each of the output latches. All incoming data lines (E44 through E51) are connected to the data input lines of output latch 2; the four lower ones (E44 through E47) are connected to the four input lines used on output latch 1. All outgoing data lines (E52 through E59) are connected to the eight input lines of each of the input buffers.

All the lines from output port 25H and input ports 21H and 25H are connected to the I/O connector.

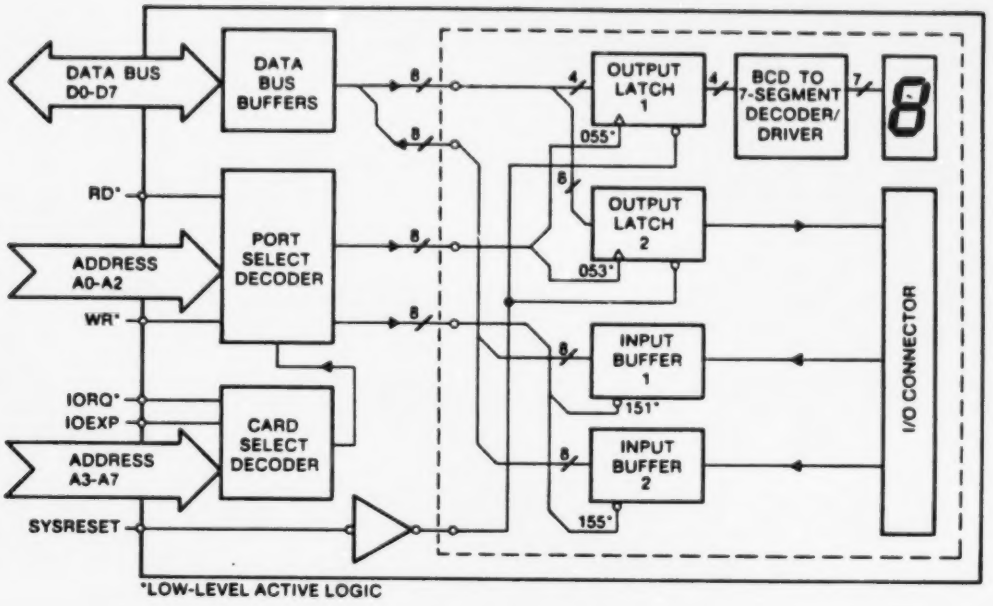


Figure 3-1. Application Example Block Diagram

Hardware

The hardware required to support this application is:

- One 7904 STD card
- Two 8-bit buffers
- Two 8-bit latches (one may be 4-bit)
- One BCD to 7-segment decoder/driver
- One 7-segment readout
- One 24-pin connector
- Four 0.01 microfarads ceramic bypass capacitors
- IC sockets as required

Construction

Two recommended breadboard techniques are wire wrapping and insulation displacement. The latter may be obtained from the 3M Company.

All connections to the existing circuits are made through the pads labeled E1 through E75. Wires may be soldered directly to these pads or individual posts for wirewrap or insulation displacement may be soldered into these pads.

Figure 3-2 is an illustration of a proposed layout. Four 0.01 microfarad capacitors are placed between VCC and Ground for noise decoupling.

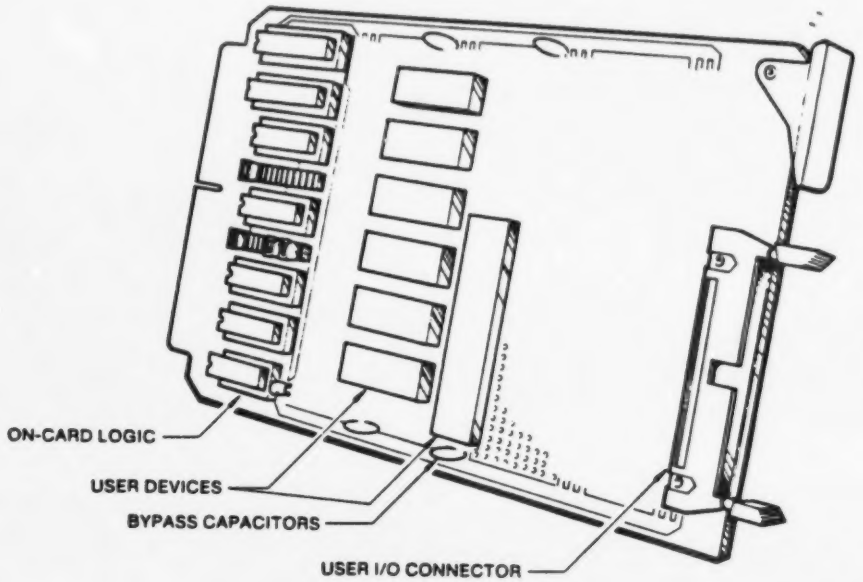


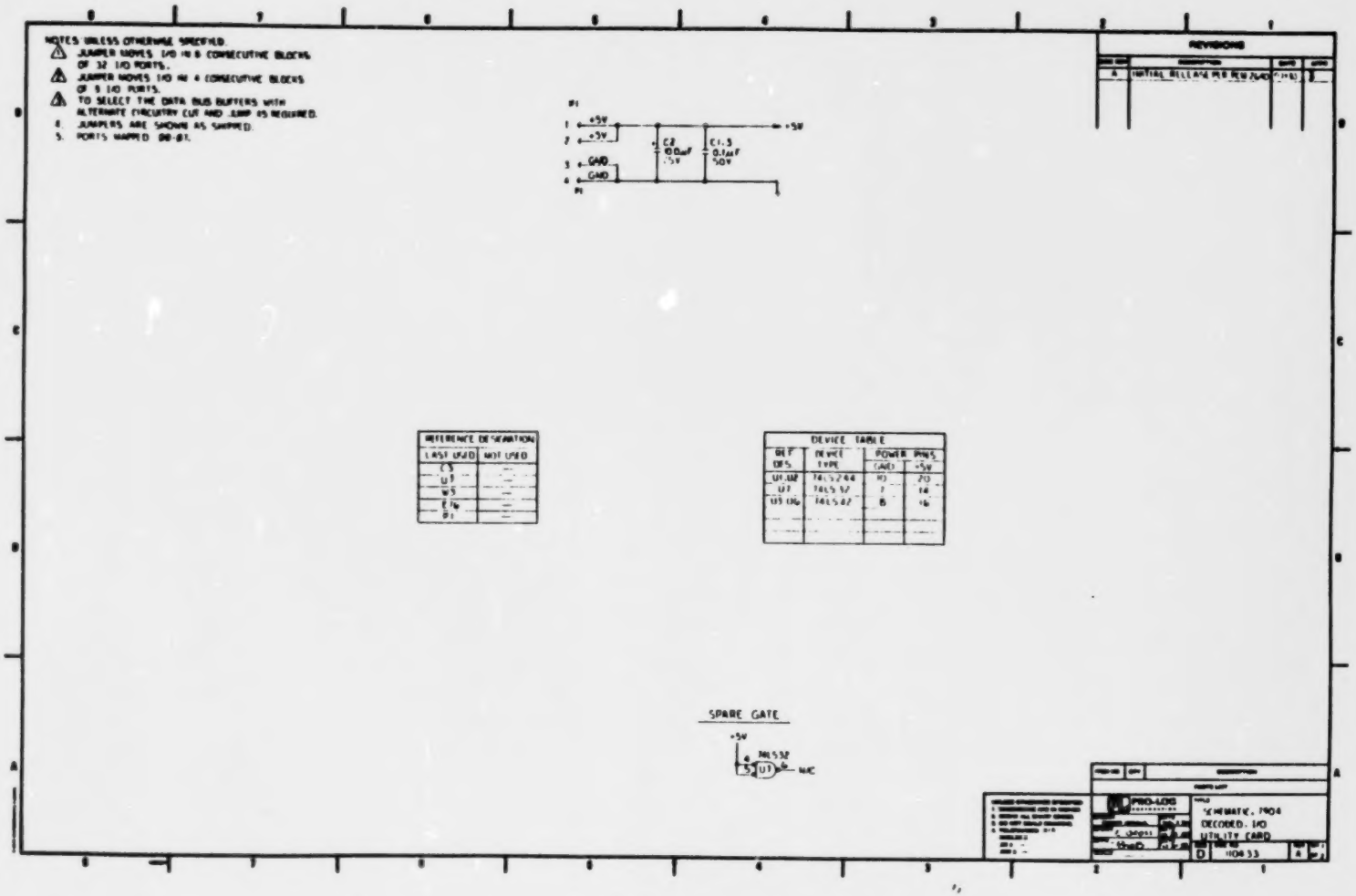
Figure 3-2. Construction Example (7904/79C04)

SECTION 5
Maintenance

REFERENCE DRAWINGS

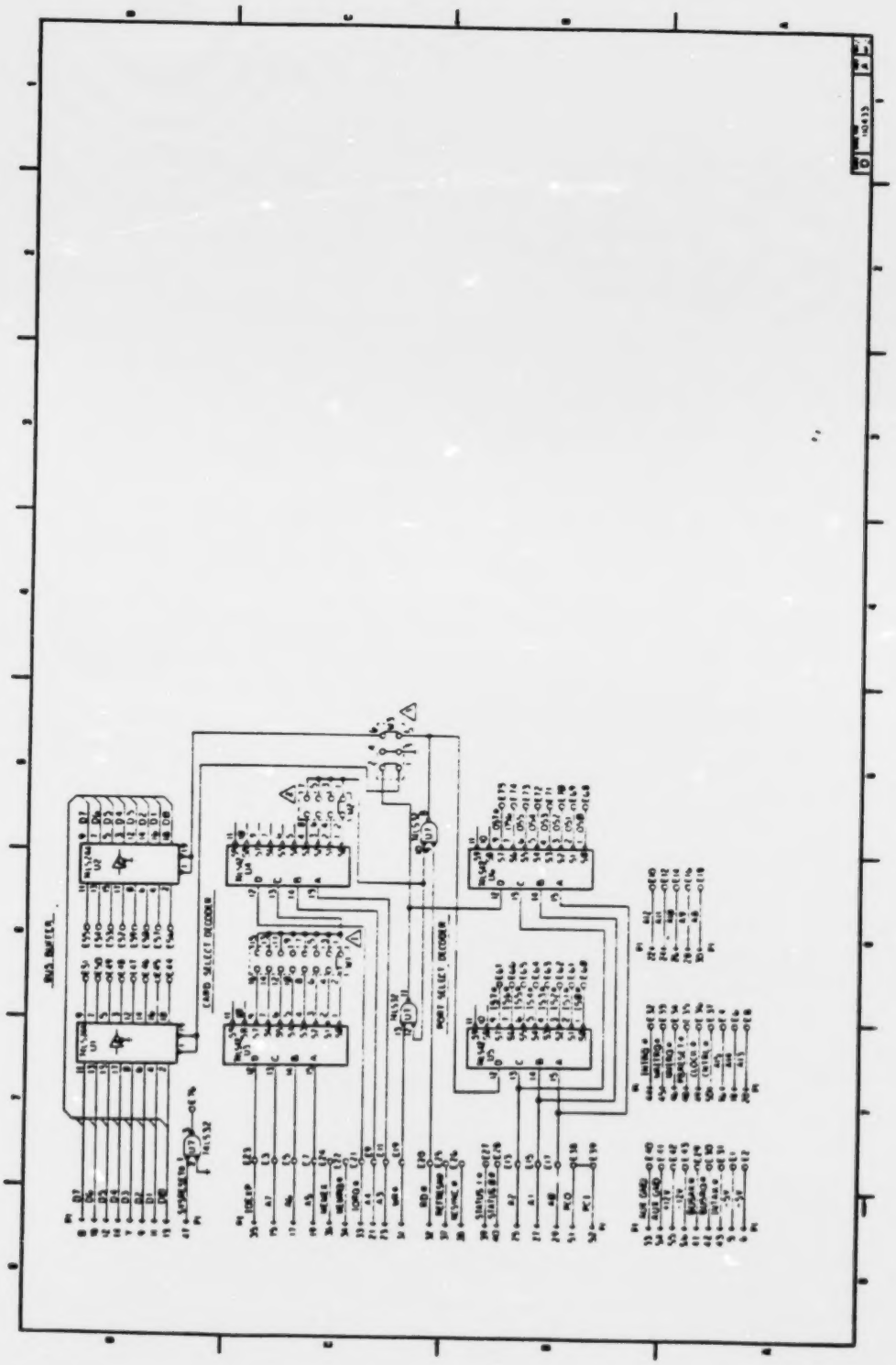
The schematics (figures 5-1 and 5-2) and assembly drawings (figures 5-3 and 5-4) in the following pages are included in this manual for **REFERENCE ONLY**. Because improvements may have been made to the card(s) since this manual was published, they may differ in some respects from the card and documentation the user received from Pro-Log.

The schematic and assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.



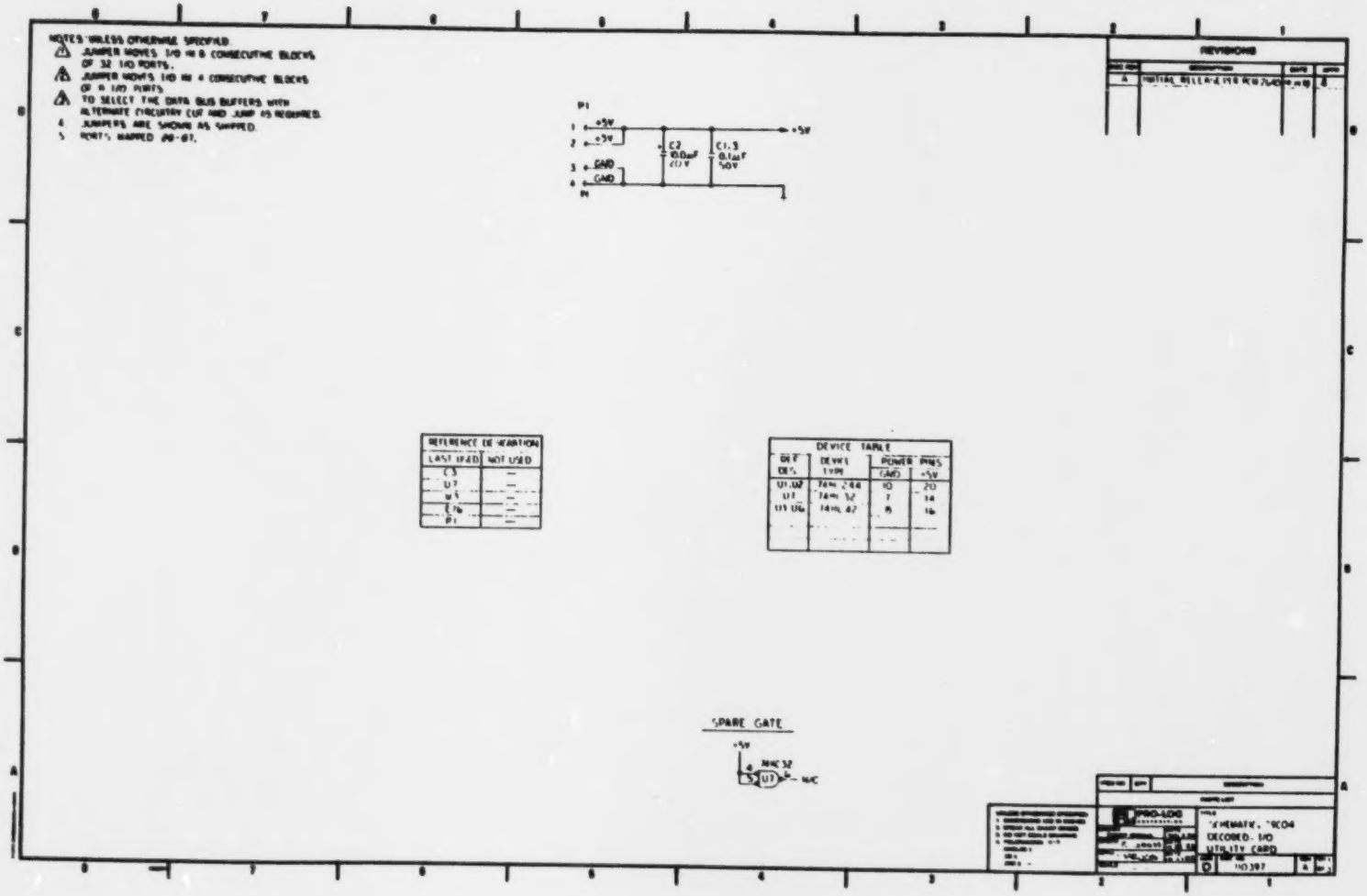
(Reference only. See documents shipped with the card.)

Figure 5-1. 7904 Schematic Page 1



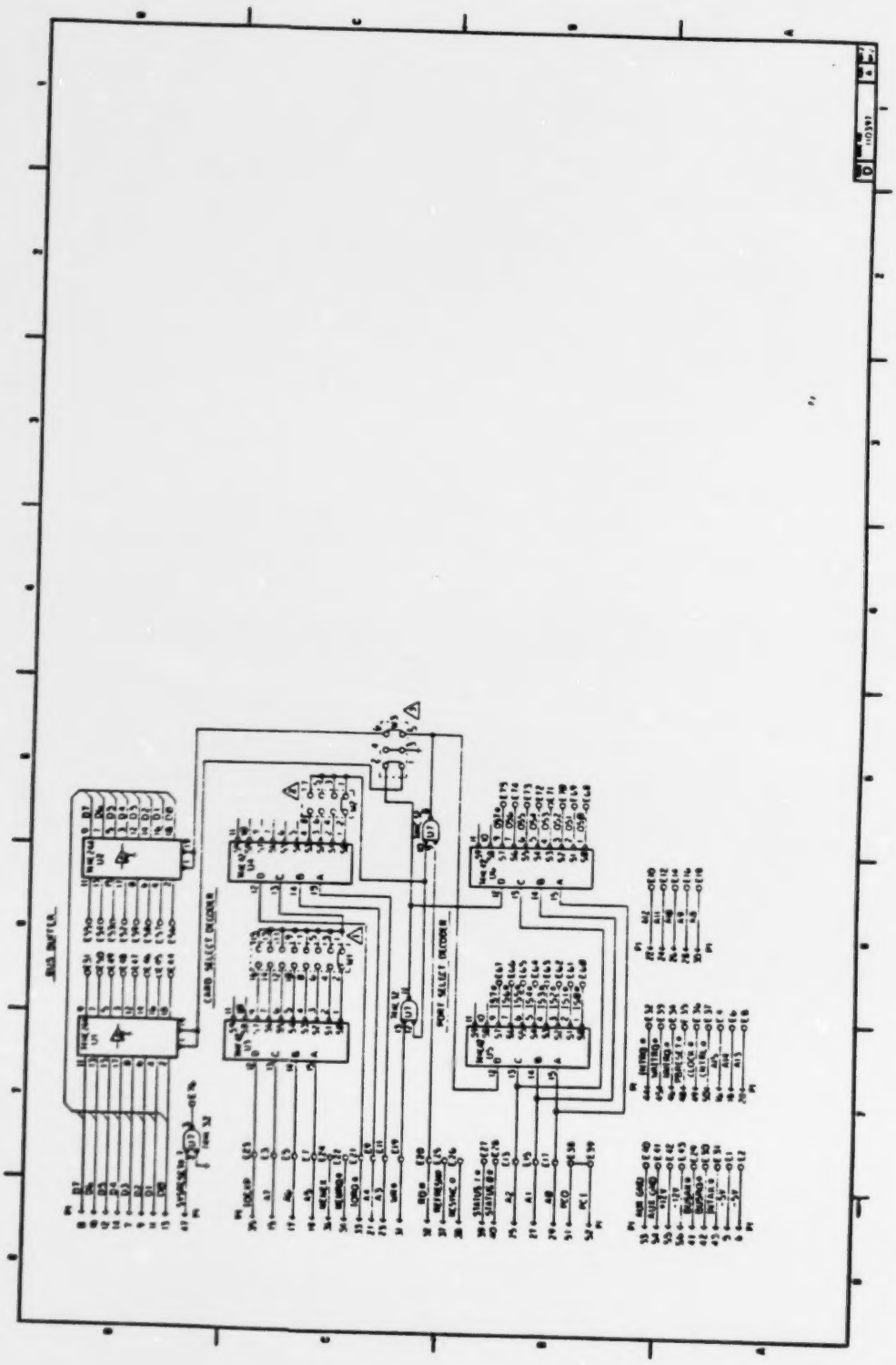
(Reference only. See documents shipped with the card.)

Figure 5-1. 7904 Schematic (continued)



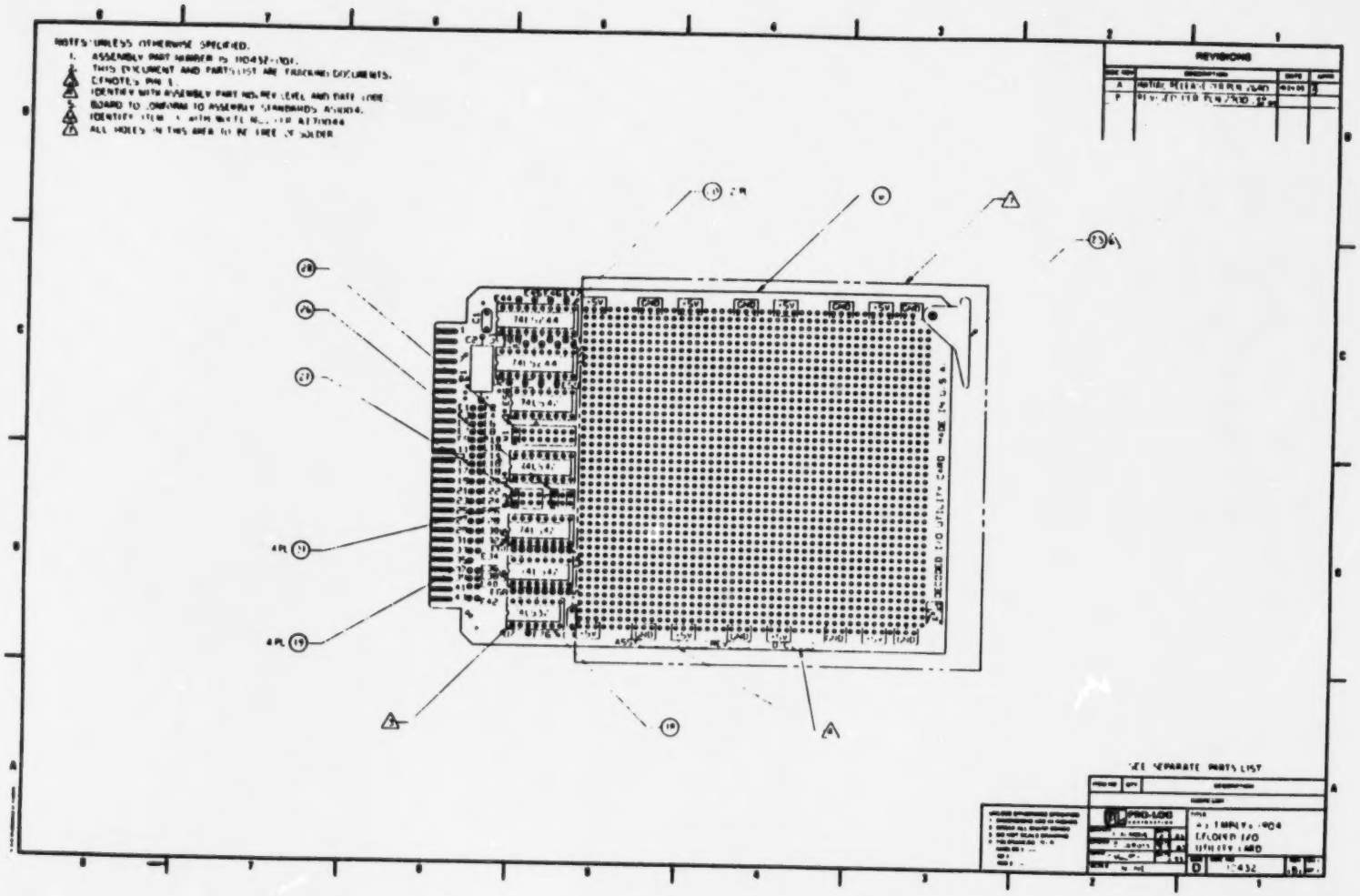
(Reference only. See documents shipped with the card.)

Figure 5-2. 79C04 Schematic



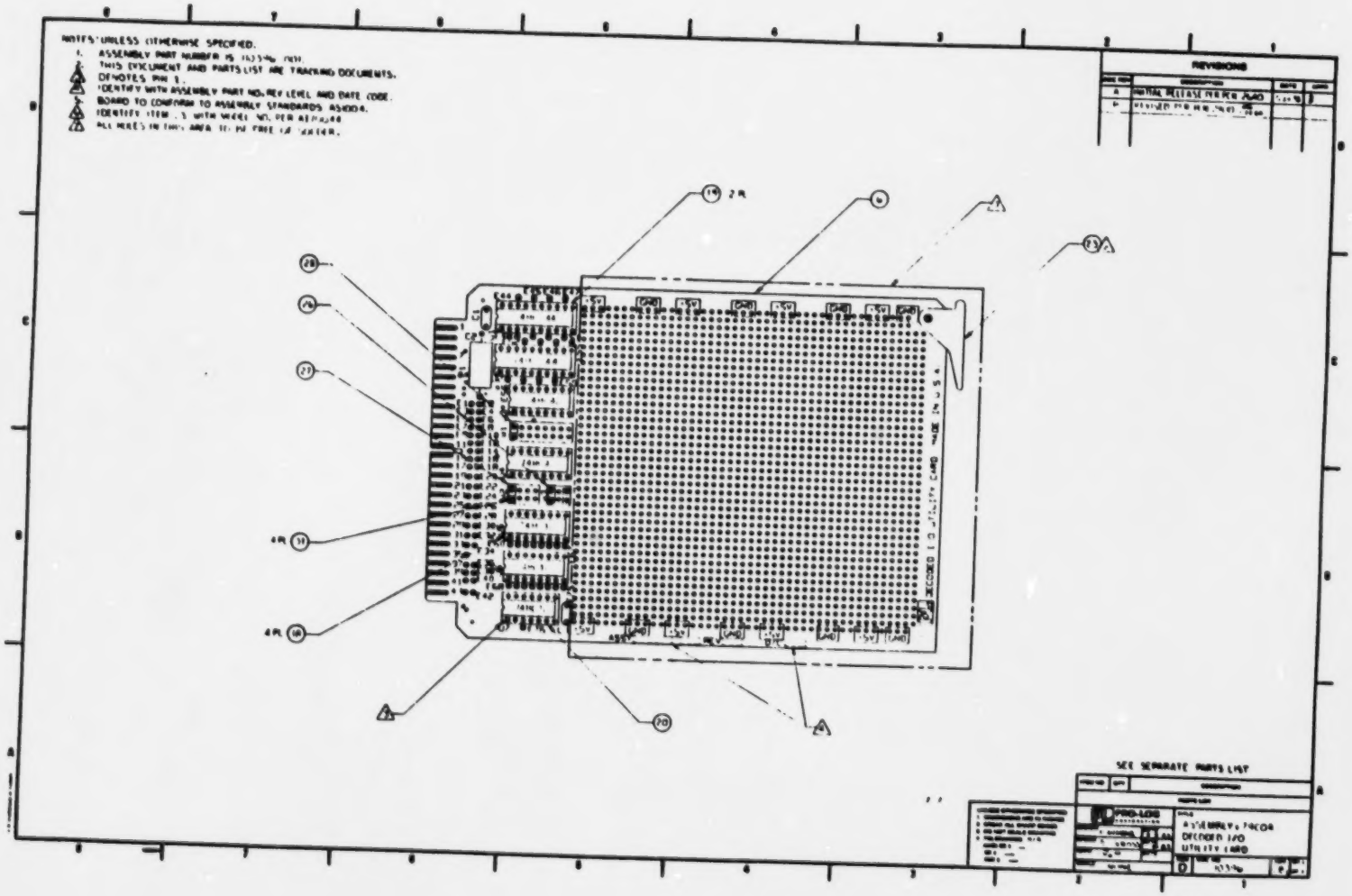
(Reference only. See documents shipped with the card.)

Figure 5-2. 79C04 Schematic (continued)



(Reference only. See documents shipped with the card.)

Figure 5-3. 7904 Assembly

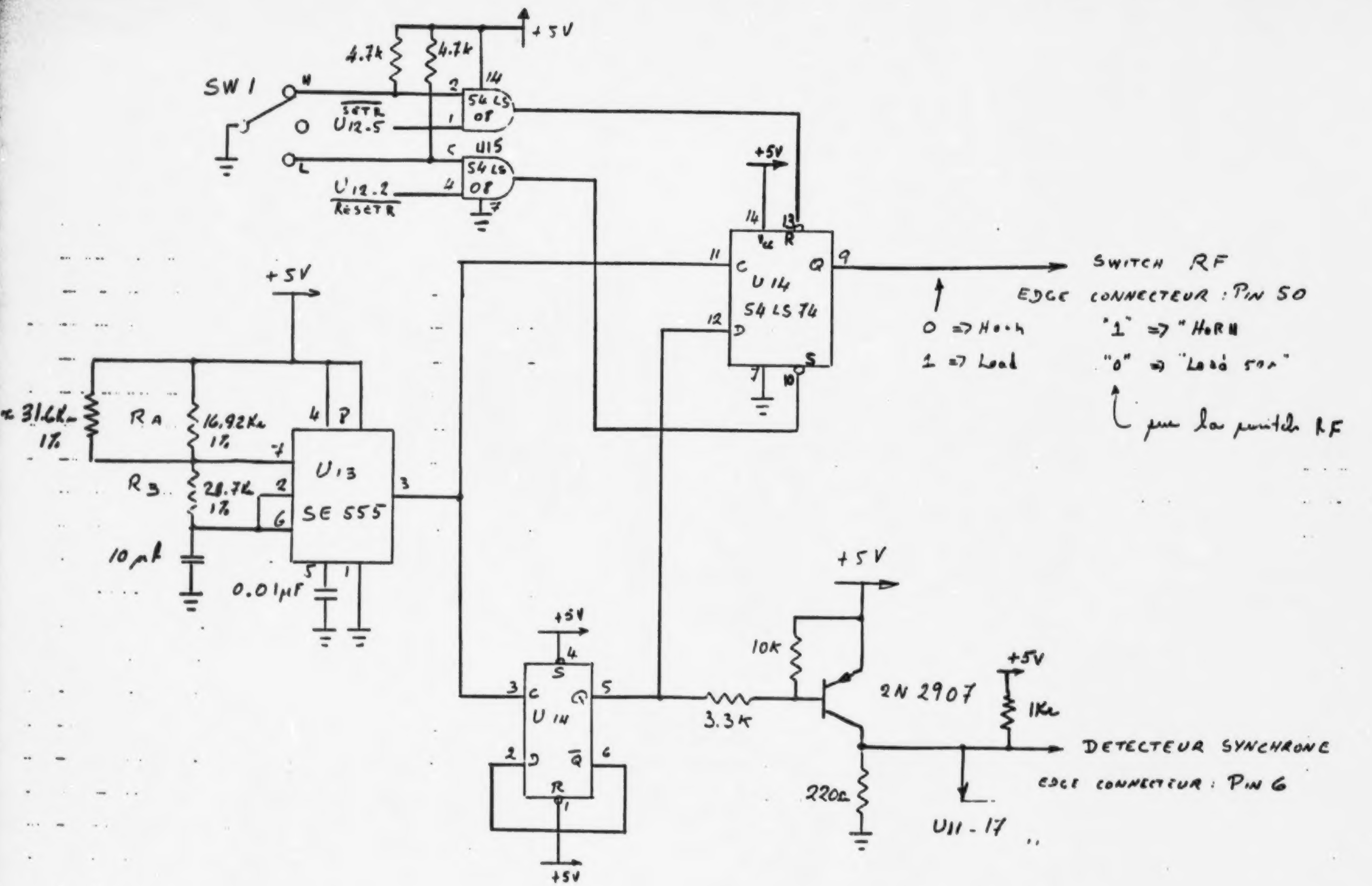


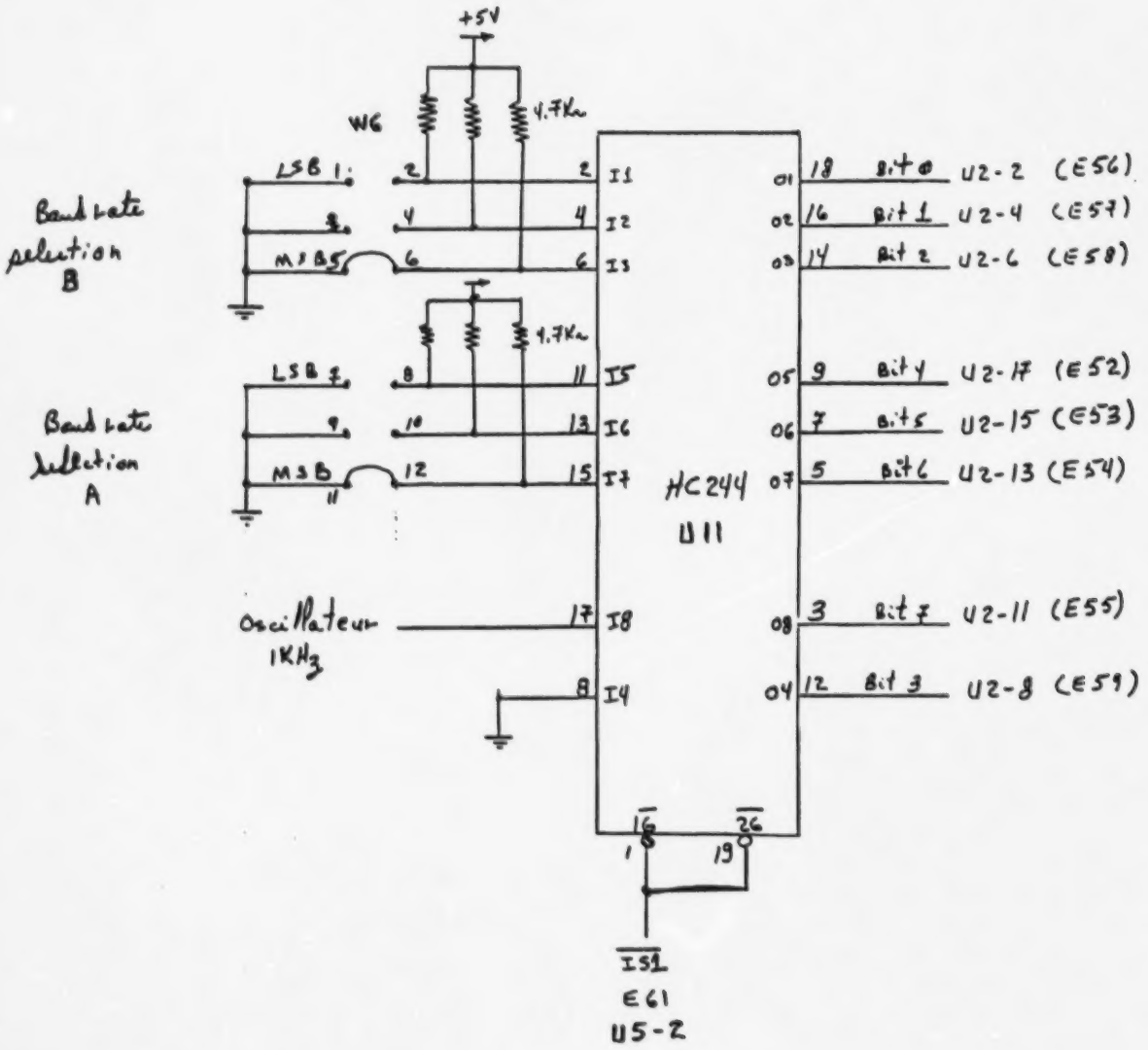
(Reference only. See documents shipped with the card.)

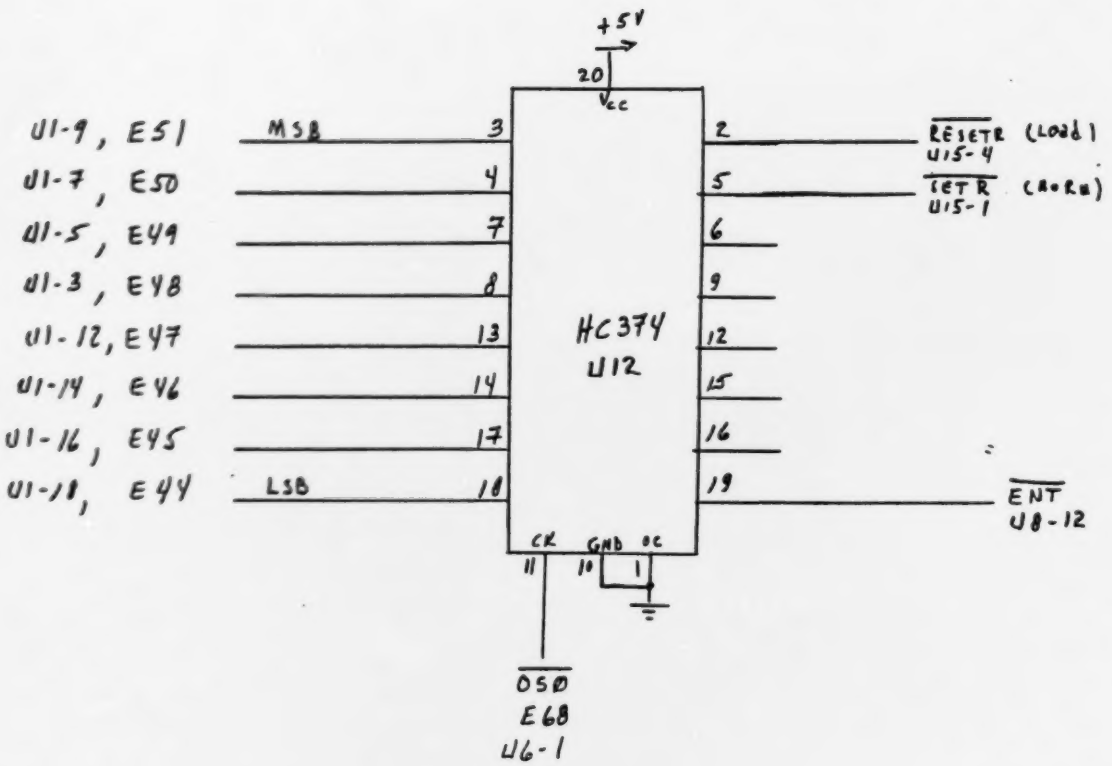
Figure 5-4. 79C04 Assembly

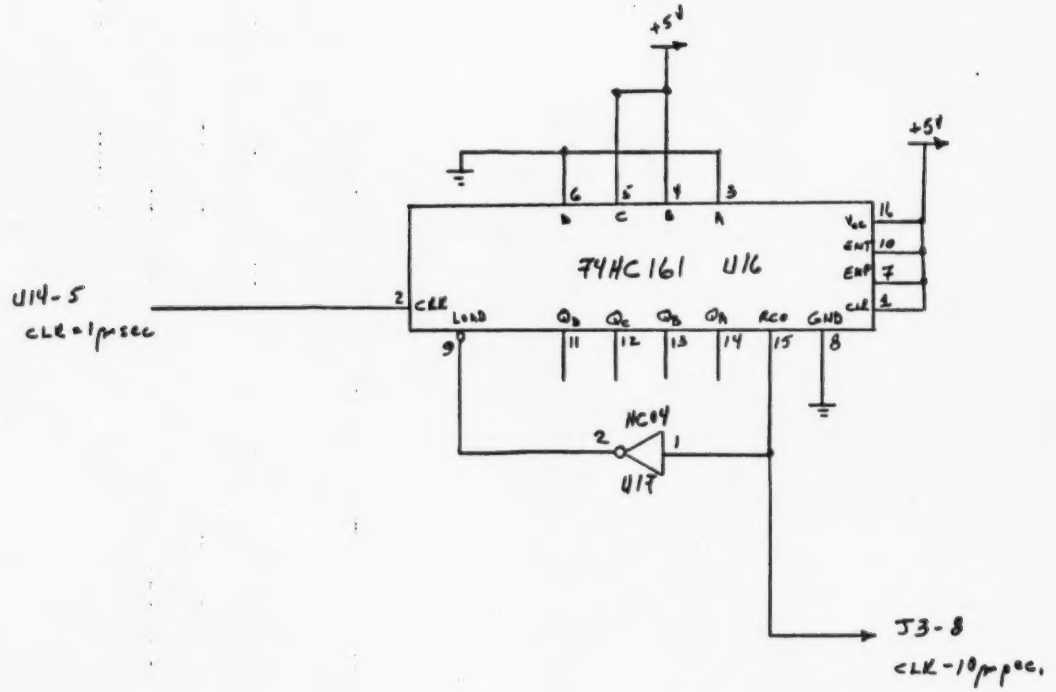
APPENDICE H.2
CIRCUITS D'ENTRÉES/SORTIES

RS-422
J3
SW1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
W1
W2
W4
W5
W6
1
50


SW 1
4.7k
4.7k
+5V
SETR U12-5
U12.2 RESETR
54 LS 08
U15
54 LS 08
+5V
U 14
54 LS 74
SWITCH RF
EDGE CONNECTEUR : PIN 50
0 => Horn
1 => Load
"1" => "HORN"
"0" => "Load 50Ω"
pour la position RF
+5V
RA
≈ 31.6kΩ 1%
16.92KΩ 1%
RB
28.7kΩ 1%
U13
SE 555
10μF
0.01μF
+5V
U 14
+5V
+5V
10K
3.3K
2N 2907
+5V
1KΩ
220Ω
DETECTEUR SYNCHRONE
EDGE CONNECTEUR : PIN 6
U11 - 17


+5V
WG
4.7Ka
LSB 1:
Baud rate selection B
MSB
4.7Ka
LSB 2
Baud rate selection A
MSB
Oscillateur 1KHz
HC244
U11
Bit 0 U2-2 (E56)
Bit 1 U2-4 (E57)
Bit 2 U2-6 (E58)
Bit 4 U2-17 (E52)
Bit 5 U2-15 (E53)
Bit 6 U2-13 (E54)
Bit 7 U2-11 (E55)
Bit 3 U2-8 (E59)
IS1
E61
U5-2


+5V
20
Vcc
U1-9, E51
MSB
3
U1-7, E50
4
U1-5, E49
7
U1-3, E48
8
U1-12, E47
13
U1-14, E46
14
U1-16, E45
17
U1-18, E44
LSB
18
HC374
U12
2
RESETR (LOAD)
U15-4
5
SETR (A+B=0)
U15-1
6
9
12
15
16
19
ENT
U8-12
CK
11
GND
10
OC
1
OSD
E68
U6-1


+5V
+5V
74HC161 U16
U14-5
CLK=1μsec
CLR
LOAD
GND
RCO
ENT
ENP
CLK
NC04
U17
J3-8
CLK-10μsec.

Interface

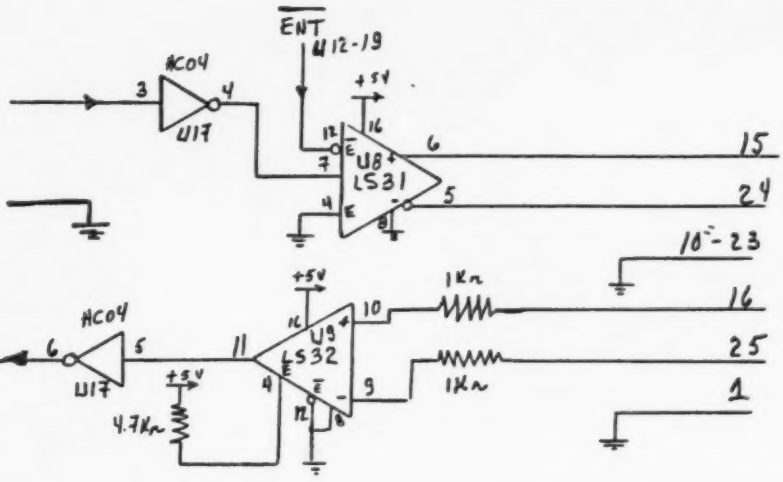
DTE

Carte 73C04

J3 - 3

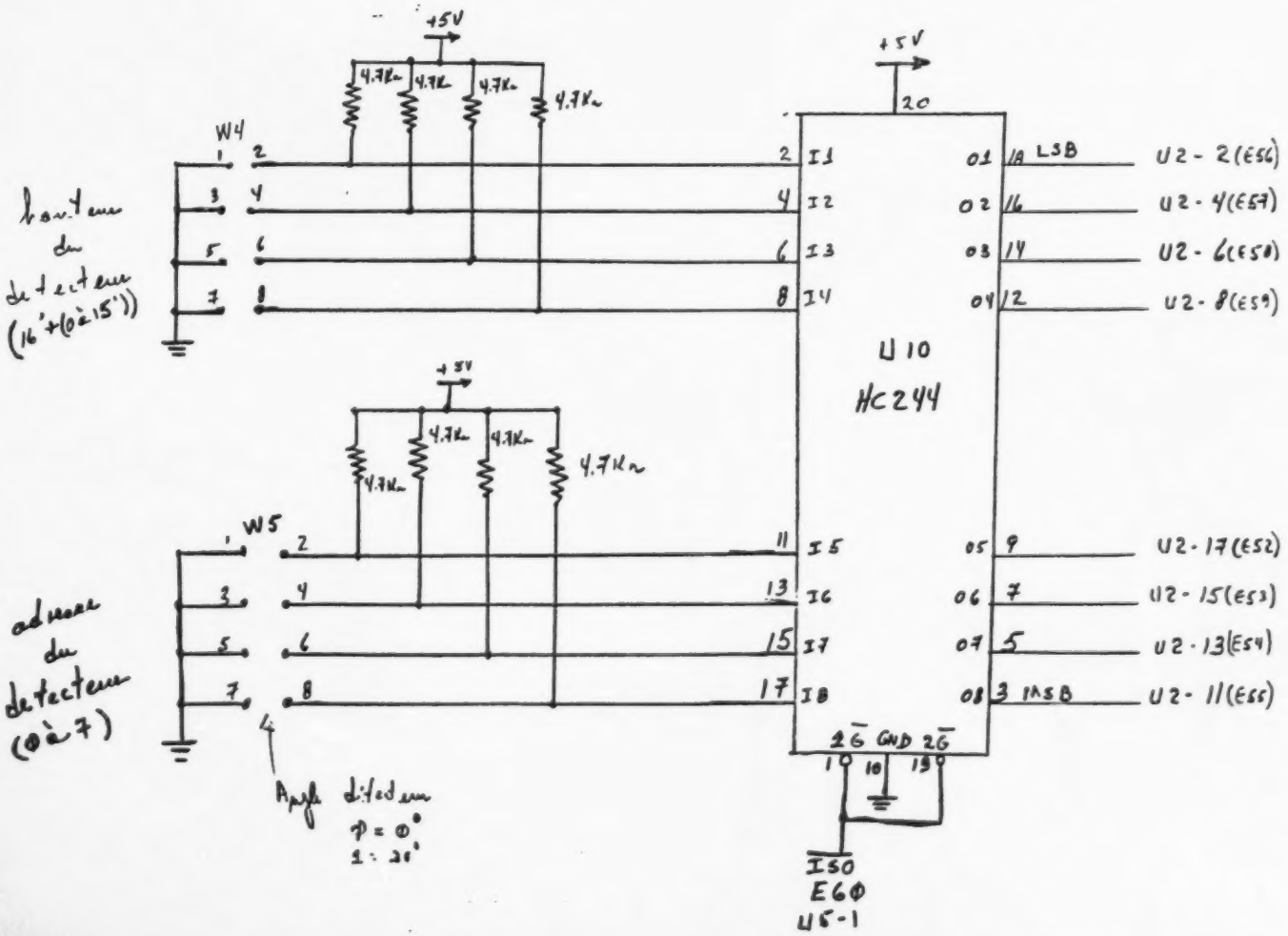
J3 - 13

J3 - 5



J2
RS-422

15 Send Data +
24 Send Data −
10-23 Signal Ground
16 Receive Data +
25 Receive Data −
1 chassis ground



Nombre de détecteurs (16' + (0 à 15'))

Adresse du détecteur (Ø à 7)

APPENDICE I

LOGICIEL: SENSEUR DE VÉHICULES

CRIQ

```
ISIS-II PL/M-80 V4.0 COMPILATION OF MODULE SENSEURVEHICULE
OBJECT MODULE PLACED IN :F1:VEHICU.OBJ
COMPILER INVOKED BY:  PLM80 :F1:VEHICU.PLM DATE(09 AVR 86) DEBUG


                $TITLE('SENSEUR DE VEHICULES  ALGO.RG  VER.2.3          ')
                $PAGEWIDTH(80)
                /*          PROGRAMME: SENSEUR DE VEHICULE            6-4417
                                       04 AVRIL  1986
                                        ROGER GARCEAU                */
  1             SENSEUR$VEHICULE:      DO;
                    /*   MEMOIRE  */
  2   1             DECLARE DEBUT$RAM LITERALLY '2000H';
  3   1             DECLARE FIN$RAM LITERALLY ' 27FFH';
  4   1             DECLARE DEBUT$ROM LITERALLY '0';
                    /*   CARTE 79C04: RS-422,CONTROLE RADIOMETRE  */
  5   1             DECLARE ADD$HAUT$ADD$DETECT LITERALLY '0';
  6   1             DECLARE ADD$ANGLE$DETECT LITERALLY '0';
  7   1             DECLARE ADD$BAUD$RATE LITERALLY '1';
  8   1             DECLARE ADD$RADIO$CONT LITERALLY '0';
  9   1             DECLARE ADD$ENABLE$422 LITERALLY '0';
 10   1             DECLARE HAUTEUR$BASE LITERALLY '16';
 11   1             DECLARE DETECT$ADD$BASE LITERALLY '30H';
                    /*     ANGLE:BIT 8 DU PORT 01 ,0:ANGLE DE 0 DEGREE ,
                           1:ANGLE DE 30 DEGREE     */
 12   1             DECLARE ANGLE$30 LITERALLY '80H';
                    /*     ENABLE TRANSMETTEUR 422:BIT 0 DU PORT 00, 0:ENABLE,
                           1:DISABLE */
 13   1             DECLARE ENTRANS$422 LITERALLY '0FEH';
 14   1             DECLARE DISTRANS$422 LITERALLY '0FFH';
                    /*CONTROLE DU RADIOMETRE: PORT 00 BIT 6:0 SELECTION DE
                      L'ANTENNE , BIT 7:0 SELECTION DE LA CHARGE, BIT 6 ET
                       BIT 7 = 1 :FONCTION NORMALE DU RADIOMETRE */
 15   1             DECLARE SELECT$HORN LITERALLY '1011$1111B';
 16   1             DECLARE SELECT$LOAD LITERALLY '7FH';
 17   1             DECLARE SELECT$RADIOM$NORM LITERALLY '0FFH';
                    /*     CARTE  MCM-CLK     */
 18   1             DECLARE CLK$T$SEC LITERALLY '40H';
 19   1             DECLARE CLK$H$SEC LITERALLY '41H';
 20   1             DECLARE CLK$SEC LITERALLY '42H';
 21   1             DECLARE CLK$MIN LITERALLY '43H';
 22   1             DECLARE CLK$HOURS LITERALLY '44H';
 23   1             DECLARE CLK$DAY$WEEK LITERALLY '45H';
 24   1             DECLARE CLK$DAY$MONTH LITERALLY '46H';
 25   1             DECLARE CLK$MONTH LITERALLY '47H';
 26   1             DECLARE CLK$INTERRUPT$STATUS LITERALLY '50H';
 27   1             DECLARE CLK$INTERRUPT$CONT LITERALLY '51H';
 28   1             DECLARE CLK$COUNTERS$RESET LITERALLY '52H';
 29   1             DECLARE CLK$RAM$RESET LITERALLY '53H';
                    /*     STATUS BIT PORT 54H,BIT 1=0 :READ OK ,
                            BIT 1=1 :ERREUR RIPPLING DES COMPTEURS  */
 30   1             DECLARE CLK$STATUS$BIT LITERALLY '54H';
 31   1             DECLARE CLK$GO$COMMAND LITERALLY '55H';
 32   1             DECLARE BCD$BASE LITERALLY '30H';
                    /*         CARTE  A/D         */
 33   1             DECLARE TEMPERATURE LITERALLY '0';
```

```
 34   1          DECLARE RADIOMETRE LITERALLY '7';
 35   1          DECLARE MUX$ADDR LITERALLY '3CH';
 36   1          DECLARE A$D$LOW$BYTE LITERALLY '3DH';
 37   1          DECLARE A$D$HIGH$BYTE$STATUS LITERALLY '3EH';
 38   1          DECLARE A$D$BUSY LITERALLY 'B0H';
                 /*      0 VOLT=20 DEGREE C =LECTURE B0H ,
                        1 DEGREE C = 1 STEP      */
 39   1          DECLARE TEMP$REF$20 LITERALLY 'B0H';
                 /*     CARTE COMMUNICATION  73C04        */
 40   1          DECLARE DATA$232$IN LITERALLY '0E1H';
 41   1          DECLARE DATA$422$IN LITERALLY '0E3H';
 42   1          DECLARE STATUS$232 LITERALLY '0E2H';
 43   1          DECLARE STATUS$422 LITERALLY '0E4H';
 44   1          DECLARE BAUD$RATE LITERALLY '0E0H';
 45   1          DECLARE DATA$232$OUT LITERALLY '0E1H';
 46   1          DECLARE DATA$422$OUT LITERALLY '0E3H';
 47   1          DECLARE COMM$CONT$232 LITERALLY '0E2H';
 48   1          DECLARE COMM$CONT$422 LITERALLY '0E4H';
                 /* RS232 : 2 STOP BITS =00, PARITY ODD =0 ,PARITY ENABLE = 1 ,
                    7 BITS PAR CHARACTERES =10 , ASYNC MODE = 10
                          -   1101$1010 B          */
 49   1          DECLARE CONTROL$BYTE$232 LITERALLY '0DAH';
                 /*  RS422 : 1 STOP BIT =01 LE RESTE COMME RS232
                       DONC -  0101$1010B  */
 50   1          DECLARE CONTROL$BYTE$422 LITERALLY '5AH';
                 /*  RS232 COMMAND BYTE : SET RTS=BIT 5=1 ,RECEIVE INACTIVE
                     BIT 2=0 ,DTR SET =BIT 1=1 ,TRANSMIT ENABLE=BIT 0=1
                     - 0010$0011B   -  */
 51   1          DECLARE COMM$BYTE$232 LITERALLY '23H';
                 /*   RS422 COMMAND BYTE : SET RTS=BIT 5=1 ,RECEIVE ACTIVE
                      =BIT 2=1 ,DTR SET=BIT 1=1 ,TRANSMIT ENABLE=BIT 0=1
                        -  0010$0111B  -       */
 52   1          DECLARE COMM$BYTE$422 LITERALLY '27H';
 53   1          DECLARE COMM$BYTE$RESET$422 LITERALLY '37H';
 54   1          DECLARE BELL LITERALLY '07H';
 55   1          DECLARE SPACE LITERALLY '20H';
 56   1          DECLARE LF LITERALLY '0AH';
 57   1          DECLARE CR LITERALLY '0DH';
 58   1          DECLARE SLASH LITERALLY '2FH';
 59   1          DECLARE SOH LITERALLY '01H';
 60   1          DECLARE ENQ LITERALLY '05H';
 61   1          DECLARE ETX LITERALLY '03H';
 62   1          DECLARE EOT LITERALLY '04H';
 63   1          DECLARE STX LITERALLY '02H';
                 /*  QUEUE INFORMATION : 204 BYTES MAX. INFORMATION
                     SOUS LA FORME  HHMMLV  - 6 BYTES PAR VEHICULE -          */
 64   1          DECLARE POINTEUR$MAX$QUEUE LITERALLY '204';
                 /*   QUEUE POUR DETECTION DES VEHICULES: 200 BYTES MAX.
                      INFORMATION SOUS LA FORME  HMLV
                        - 4 BYTES PAR VEHICULES -       */
 65   1          DECLARE POINTEUR$MAX$VEHICULE$DETECTE LITERALLY '200';
```

```
                $EJECT
                    /*
                                DECLARATION    DES    VARIABLES
                                ------------------------------      */
 66   1             DECLARE MATRICE$CUMUL (5) STRUCTURE (V (6) ADDRESS);
 67   1             DECLARE MATRICE$INTER (5) STRUCTURE (V (6) ADDRESS);
 68   1             DECLARE (T$ACTUEL,VITESSE,DETECT$DEBUT$VEH,CAS$SATURE,LONGEUR)
          -          BYTE;
 69   1             DECLARE (NB$MESURE,J,K,MAX,SEUIL$TB,VREF,SPEED,L,ETAT,SEUIL) B
          -          YTE;
 70   1             DECLARE TEMP$AMB (10) BYTE;
 71   1             DECLARE REC$BUFFER (56) BYTE;
 72   1             DECLARE (TR,TF,TB,TA) ADDRESS;
 73   1             DECLARE YEAR (2) BYTE;
 74   1             DECLARE ETAT$ROUTE (48) BYTE;
 75   1             DECLARE (DETECTION$FIN$VEHICULE,H$CAMION,H$AUTO,DETECT$ADD) BY
          -          TE;
 76   1             DECLARE (ANGLE,BAUD$RATE$422$232,TEMP,MIN$CLK,HEURE) BYTE;
 77   1             DECLARE (POINTEUR$ETAT$ROUTE,TEMP$LOCAL) BYTE;
 78   1             DECLARE BUFFER$232 (15) BYTE;
 79   1             DECLARE QUEUE$INFO (204) BYTE;
 80   1             DECLARE VEHICULE$DETECTE (200) BYTE;
 81   1             DECLARE (I,POINTEUR$REC,ERROR,REC$COMPLETE,MESSAGE,REC$PERMISS
          -          ION) BYTE;
 82   1             DECLARE (POINTEUR$ECRITURE$QUEUE,POINTEUR$LECTURE$DEBUT$QUEUE)
          -          BYTE;
 83   1             DECLARE (POINTEUR$LECTURE$FIN$QUEUE,POINTEUR$ECRITURE$VEHICULE
          -          ) BYTE;
 84   1             DECLARE (POINTEUR$LECTURE$VEHICULE,MIN,LECTURE$V$AD,LPC) BYTE;
 85   1             DECLARE TRANS$BUFFER (48) BYTE;
 86   1             DECLARE (G,ETAT$R,T$MIN) BYTE;
 87   1             DECLARE GAIN(17) BYTE DATA (245,156,98,63,41,27,18,8,0,
                                  98,96,95,94,96,96,97,97);
 88   1             DECLARE (ETAT$SEC,ETAT$MOUILLE,ETAT$GLAE$NEIGE) BYTE DATA (26,
          -          52,52);
 89   1             DECLARE (TRESHOLD$SEUIL,TRESHOLD$NEGATIF,SEUIL$SATURE) BYTE;
 90   1             DECLARE (TN,TC) BYTE;
```

```
$EJECT
   /*
                IDENTIFICATION DES VARIABLES
                ----------------------------
        MAX : VOLTAGE MAX. DETECTE
        SEUIL$TB  :SEUIL POUR DETECTER LA PENTE DESCENDANTE
        I , J : INDICE TEMPORAIRE
        VREF :VOLTAGE DE REFERENCE OU 0 DE L'APPAREIL
        TR :TEMPS DE MONTEE
        TF :TEMPS DESCENTE
        TB :TEMPS SATURATION
        TA :TEMPS TOTAL
        TN :TEMPS NEGATIF=TEMPS OU T$ACTUEL<SEUIL-TRESHOLD$NEGATIF
            EN CONTINUE
        TC :TEMPS DE COMPENSATION DU AU TRESHOLD SUR LES PENTES
        TRESHOLD$SEUIL :TRESHOLD POUR ELIMINER LE BRUIT ET POUR
                        DETECTION
        TRESHOLD$NEGATIF :SEUIL EMPECHANT LE FILTRE DE FONTIONNER
                          EN NEGATIF
        SEUIL$SATURE :SEUIL DETERMINANT SI LE VEHICULE EST DANS
                      LE CAS SATURATION OU NON
        ETAT$SEC :SEUIL DETERMINANT L'ETAT SEC DE LA CHAUSSEE
        ETAT$MOUILLE :SEUIL DETERMINANT L'ETAT MOUILLE DE
                      LA CHAUSSEE
        ETAT$GLACE$NEIGE :SEUIL DETERMINANT L'ETAT GLACE DE
                          LA CHAUSSEE
        ETAT :ETAT DE LA CHAUSSEE
        SEUIL :NIVEAU OU TEMP. ACTUEL DE LA CHAUSSEE SANS VEHICULE
        H$CAMION ET H$AUTO :HAUTEUR ENTRE RADIOMETRE ET VEHICULE
        DECTECT$ADD :NO. DU DETECTEUR (0 A 7)
        TEMP$LOCAL :TEMPERATURE INTERNE DE LA BOITE
        POINTEUR$REC :INDICE 0 A 55 POUR REC$BUFFER
        ERROR : 0=NO ERROR
        REC$COMPLETE : 0FFH==MESSAGE RECU EN ENTIER
        MESSAGE :NO. INDIQUANT LE GENRE DE MESSAGE VALIDE RECU
        REC$PERMISSION :0FFH= OK PEUT RECEVOIR UN AUTRE MESSAGE
        QUEUE$INFO( ) :HHMMLV
        VEHICULE$DETECTE( ) :HMLV
        MIN :COMPTEUR DES MIN. POUR DETECTE LES 30 MIN.
        SPEED :CATEGORIE DE VITESSE DU VEHICULE 0 A 4
        L :CATEGORIE DE LONGEUR DU VEHICULE 0 A 4
        LECTURE$V$AD : SI = 1 = LECTURE TEMPERATURE INTERNE
                       OU VREF
        G :GAIN A APPLIQUER A LA LECTURE DU A-D. CETTE VALEUR
           EST FONCTION DE LA TEMPERATURE AMBIANTE
        GAIN(-) :TABLE DU GAIN A APPLIQUER EN FONCTION DE LA
                 TEMPERATURE AMBIANTE. GAIN(0): GAIN A -40 C.
                 .... GAIN(16): GAIN A +40 C.
        ETAT$R :ETAT LE PLUS DANGEREUX DEPUIS LE DEBUT DE LA
                PRESENTE DEMI-HEURE
                   */
```

```
                $EJECT
                    /*
                                INITIALISATION
                                --------------      */
 91   1             INITIALISATION: PROCEDURE;
 92   2             DO;
 93   3             DECLARE (TEMP,I,K) BYTE;
                    /*  CARTE 7904 DISABLE TRANSMIT 422 ,CONTROLE RADIOMETRE
                        NORMAL */
 94   3             OUTPUT (ADD$RADIO$CONT)=0FFH;
                    /* CARTE 79C04 LECTURE PARAMETRES:HAUTEUR,ADRESSE,ANGLE */
 95   3             TEMP=INPUT(ADD$HAUT$ADD$DETECT);
 96   3             H$AUTO=(TEMP AND 0FH) + HAUTEUR$BASE;
 97   3             DETECT$ADD=SHR((TEMP AND 70H),4);
 98   3             DETECT$ADD=DETECT$ADD + DETECT$ADD$BASE;
 99   3             ANGLE=TEMP AND B0H;
                    /* LECTURE SELECTION DU BAUD RATE  */
100   3             BAUD$RATE$422$232=INPUT(ADD$BAUD$RATE) AND 77H;
                    /* INTIALISATION CARTE MCM-CLK   */
                    /* AUCUNE INTURRUPTION HARWARE MAIS FLAGS A TOUTES LES MIN.
                        ET A TOUTES LES HEURES      */
101   3             OUTPUT(CLK$INTERRUPT$CONT)=0;
                    /* RESET A 0 DE L'HORLOGE ET RAM   */
102   3             OUTPUT(CLK$RAM$RESET)=0FFH;
103   3             OUTPUT(CLK$COUNTERS$RESET)=0FFH;
104   3             OUTPUT(CLK$60$COMMAND)=0FFH;
                    /*  MISE A 0 DE L'ANNEE   */
105   3             YEAR(0),YEAR(1)=0;
                    /* MISE A 0 DU COMPTEUR DE  5 MINUTES    */
106   3             T$MIN=0;
                    /*   INITIALISATION CARTE A/D     */
                    /*                                */
107   3             OUTPUT(MUX$ADDR)=RADIOMETRE;
                    /*   INITIALISATION INTERFACE COMMUNICATION   */
108   3                 DO I=0 TO 2;
109   4                     OUTPUT(COMM$CONT$232)=0;
110   4                     OUTPUT(COMM$CONT$422)=0;
111   4                 END;
                    /*    RESET INTERFACE    */
112   3             OUTPUT(COMM$CONT$232)=40H;
113   3             OUTPUT(COMM$CONT$422)=40H;
                    /*   CONTROL BYTE UART    */
114   3             OUTPUT(COMM$CONT$232)=CONTROL$BYTE$232;
115   3             OUTPUT(COMM$CONT$422)=CONTROL$BYTE$422;
                    /*     COMMAND BYTE TO UART   */
116   3             OUTPUT(COMM$CONT$232)=COMM$BYTE$232;
117   3             OUTPUT(COMM$CONT$422)=COMM$BYTE$422;
                    /*  BAUD RATE SELECTION  */
118   3             OUTPUT(BAUD$RATE)=BAUD$RATE$422$232;
                    /*   INITIALISATION  DES VARIABLES DU BUFFER$232   */
119   3             BUFFER$232(0)=BELL;
120   3             BUFFER$232(3)=SLASH;
121   3             BUFFER$232(6),BUFFER$232(10)=SPACE;
122   3             BUFFER$232(13)=LF;
123   3             BUFFER$232(14)=CR;
                    /*   INTIALISATION DES VARIABLES DE RECEPTION  */
124   3             POINTEUR$REC=0;
```

```
 125   3          REC$COMPLETE=0;
 126   3          ERROR=0;
                  /* MATRICES DES RESULTATS A 0  */
 127   3          DO I=0 TO 4;
 128   4              DO K=0 TO 5;
 129   5                  MATRICE$INTER(I).V(K)=0;
 130   5                  MATRICE$CUMUL(I).V(K)=0;
 131   5              END;
 132   4            END;
                  /*  ETAT DE LA ROUTE INITIALISEE A ?  */
 133   3          ETAT$R=0;
 134   3          POINTEUR$ETAT$ROUTE=0;
 135   3          DO I=0 TO 47;
 136   4              ETAT$ROUTE(I)='?';
 137   4            END;
                  /*  QUEUE D'INFORMATION       */
 138   3          POINTEUR$ECRITURE$QUEUE=0;
 139   3          POINTEUR$LECTURE$DEBUT$QUEUE=0;
 140   3          POINTEUR$LECTURE$FIN$QUEUE=0;
                  /*   QUEUE DE VEHICULE DETECTEE    */
 141   3          POINTEUR$ECRITURE$VEHICULE=0;
 142   3          POINTEUR$LECTURE$VEHICULE=0;
                  /*  INITIALISATION DES PARAMETRES FONCTION DE LA HAUTEUR
                       DU DETECTEUR  */
                  /*  SEUIL SATURE A 16 PIEDS=52=2.03V,DIMINUE DE 6 STEPS PAR
                      PIED A 20 PIEDS=28=1.09V,PUIS A 21 PIEDS=25=.98V ET
                      DIMINUE DE 3 STEPS PAR PIED . A 24 PIEDS=16=.625V
                                 */
 143   3          TEMP=H$AUTO-HAUTEUR$BASE;
 144   3          IF TEMP>4 THEN SEUIL$SATURE=40-(TEMP*3);
 146   3                    ELSE SEUIL$SATURE=52-(TEMP*6);
                  /*TRESHOLD$SEUIL A 16 PIEDS=14=.55V,A 20 PIEDS=6=0.23V,
                      A 24 PIEDS=4=.15V */
 147   3          IF TEMP>4 THEN TRESHOLD$SEUIL=5;
 149   3          IF TEMP>6 THEN TRESHOLD$SEUIL=4;
 151   3          IF TEMP<=4 THEN TRESHOLD$SEUIL=14-(SHL(TEMP,1));
                  /* TRESHOLD$NEGATIF=TRESHOLD$SEUIL*2      */
 153   3          TRESHOLD$NEGATIF=SHL(TRESHOLD$SEUIL,1);
                  /*  CALCUL HAUTEUR ENTRE DETECTEUR ET VEHICULE   */
 154   3          H$CAMION=H$AUTO - 10;
 155   3          H$CAMION=H$CAMION + SHR(H$CAMION,3);
 156   3          H$AUTO=H$AUTO-4;
 157   3          H$AUTO=H$AUTO + SHR(H$AUTO,3);
 158   3          IF ANGLE<>0 THEN DO;
 160   4              H$CAMION=H$CAMION+SHR(H$CAMION,1);
 161   4              H$AUTO=H$AUTO+SHR(H$AUTO,1);
 162   4            END;
 163   3          MAX=0;
                  /*   SEUIL INITIALISEE A -5.0 VOLTS  */
 164   3          SEUIL=0;
 165   3          DETECT$DEBUT$VEH=0;
 166   3          NB$MESURE=0;
 167   3          DO I=0 TO 9;
 168   4              TEMP$AMB(I)=0;
 169   4             END;
 170   3          J=0;
                  /*   CARTE MCM-CLK A TOUTES LES MIN. ET HEURES STATUS  */
```

```
 171   3          OUTPUT(CLK$INTERRUPT$CONT)=18H;
                  /*   RECEPTION DE MESSAGE PERMIS    */
 172   3          REC$PERMISSION=0FFH;
 173   3          END;
 174   2      END INITIALISATION;
```

```
                $EJECT
                    /*
                        PROCEDURE POUR LIRE L'HEURE ET MINUTES
                        -------------------------------------- */
175   1             READ$CLK$HHMM: PROCEDURE ;
176   2             DECLARE STATUS BYTE;
177   2             DO;
178   3             STATUS=1;
179   3             DO WHILE STATUS;
180   4                 MIN$CLK=INPUT(CLK$MIN);
181   4                 HEURE=INPUT(CLK$HOURS);
182   4                 STATUS=INPUT(CLK$STATUS$BIT);
183   4               END;
184   3             END;
185   2         END READ$CLK$HHMM;



                    /*
                        PROCEDURE POUR INSTRUCTION SIM DU 8085
                        --------------------------------------
                        CETTE PROCEDURE FAIT PARTIE DU PLM80.LIB
                                                                */
186   1             S$MASK: PROCEDURE (MASK) EXTERNAL;
187   2             DECLARE MASK BYTE;
188   2         END S$MASK;
```

```
            $EJECT
                /*
                  PROCEDURE DE FORMATION DE L'INFORMATION DANS LE BUFFER:HMLV
                  ------------------------------------------------------------
        -
                                                                            */
 189   1          FORMATION$INFO: PROCEDURE;
 190   2          DO;
 191   3          CALL READ$CLK$HHMM;
 192   3          VEHICULE$DETECTE(POINTEUR$ECRITURE$VEHICULE)=HEURE;
 193   3          VEHICULE$DETECTE(POINTEUR$ECRITURE$VEHICULE + 1)=MIN$CLK;
 194   3          VEHICULE$DETECTE(POINTEUR$ECRITURE$VEHICULE + 2)=LONGEUR;
 195   3          VEHICULE$DETECTE(POINTEUR$ECRITURE$VEHICULE + 3)=VITESSE;
 196   3          POINTEUR$ECRITURE$VEHICULE=POINTEUR$ECRITURE$VEHICULE + 4;
 197   3          IF POINTEUR$ECRITURE$VEHICULE>=POINTEUR$MAX$VEHICULE$DETECTE T
        -    HEN
 198   3                              POINTEUR$ECRITURE$VEHICULE=0;
 199   3          DETECT$DEBUT$VEH=0;
 200   3          RETURN;
 201   3          END;
 202   2      END FORMATION$INFO;
```

```
                $EJECT
                    /*
                       ROUTINE D'INTERRUPTION DE L'INTERFACE 422
                       -----------------------------------------
                       VENANT DE LA RECEPTION D'UN CARACTERE    */
 203   1          REC$422$INT: PROCEDURE INTERRUPT 6;
 204   2          DECLARE (ENTREE,STATUS) BYTE;
 205   2          DO;
 206   3          ENTREE=INPUT(DATA$422$IN);
 207   3          STATUS=INPUT(STATUS$422);
 208   3          IF REC$PERMISSION <> OFFH THEN RETURN;
 210   3          STATUS=STATUS AND 38H;
 211   3          IF STATUS <> 0 OR POINTEUR$REC>55 THEN DO;
 213   4              OUTPUT(COMM$CONT$422)=COMM$BYTE$RESET$422;
 214   4              OUTPUT(COMM$CONT$422)=COMM$BYTE$422;
 215   4              ERROR=0FFH;
 216   4              POINTEUR$REC=0;
 217   4              RETURN;
 218   4              END;
 219   3           IF ENTREE=SOH THEN DO;
 221   4              ERROR=0;
 222   4              POINTEUR$REC=0;
 223   4              END;
 224   3           REC$BUFFER(POINTEUR$REC)=ENTREE;
 225   3           POINTEUR$REC=POINTEUR$REC + 1;
 226   3           IF ENTREE=EOT THEN DO;
 228   4              REC$PERMISSION=0;
 229   4              REC$COMPLETE=0FFH;
 230   4              END;
 231   3           END;
 232   2       END REC$422$INT;
```

```
                $EJECT
                    /*
                        PROCEDURE LECTURE DU VOLTAGE   A/D
                        ---------------------------------  */
 233   1          MESURE$A$D: PROCEDURE (NUMERO);
 234   2          DECLARE (STATUS,TEMP,NUMERO) BYTE;
 235   2          DO;
 236   3          OUTPUT(MUX$ADDR)=NUMERO;
 237   3          STATUS=80H;
 238   3          DO WHILE STATUS=80H;
 239   4              STATUS=(INPUT(A$D$HIGH$BYTE$STATUS) AND 80H);
 240   4              END;
 241   3          T$ACTUEL=INPUT(A$D$LOW$BYTE);
 242   3          T$ACTUEL=SHR(T$ACTUEL,4);
 243   3          TEMP=INPUT(A$D$HIGH$BYTE$STATUS);
 244   3          TEMP=SHL(TEMP,4);
 245   3          T$ACTUEL=T$ACTUEL OR TEMP;
 246   3          END;
 247   2      END MESURE$A$D;
```

```
                $EJECT
                    /*
                       PROCEDURE POUR LIRE LE VOLTAGE DE REFERENCE OU LE 0
                       ---------------------------------------------------
                       DE L'APPAREIL
                       ------------- */
 248   1          MESURE$REF: PROCEDURE;
 249   2          DECLARE I BYTE;
 250   2          DECLARE TEMP BYTE;
 251   2          DECLARE VREF$M ADDRESS;
 252   2          DO;
 253   3          OUTPUT(ADD$RADIO$CONT)=SELECT$LOAD;
                  /* DELAIS DU AU SYSTEME:50  MSEC.  */
 254   3          DO I=1 TO 2;
 255   4              CALL TIME(250);
 256   4          END;
                  /* MOYENNE DE 5 ECHANTILLONS SUR PROCHAIN 50  MSEC. */
 257   3          VREF$M=0;
 258   3          DO I=1 TO 5;
 259   4              CALL TIME(100);
 260   4              CALL MESURE$A$D(RADIOMETRE);
 261   4              VREF$M=T$ACTUEL + VREF$M;
 262   4          END;
 263   3          OUTPUT(ADD$RADIO$CONT)=SELECT$RADIOM$NORM;
                  /* DELAIS DU AU SYSTEME:  50 M.SEC.    */
 264   3          DO I=1 TO 2;
 265   4              CALL TIME(250);
 266   4           END;
 267   3          VREF=VREF$M/5;
 268   3          END;
 269   2      END MESURE$REF;
```

```
                $EJECT
                    /*            PROCEDURE DE CALIBRATION
                                  ------------------------
                        PROCEDURE POUR CONNAITRE LA TEMPERATURE INTERNE DE LA
                        BOITE , LA MESURE DU VOLTAGE DE REFERNCE ET
                        LE GAIN A APPLIQUER.
                                */
 270    1           CALIBRATION: PROCEDURE;
 271    2           DECLARE TEMP BYTE;
 272    2           DO;
 273    3                   MIN=0;
                            /* MESURE TEMPERATURE INTERNE DE LA BOITE   */
 274    3                   LECTURE$V$AD=1;
 275    3                   CALL MESURE$A$D (TEMPERATURE);
 276    3                   TEMP$LOCAL=T$ACTUEL;
                            /*  LA TEMPERATURE A L'INTERIEUR DE LA BOITE EST
                                EGALE A 01H PAR DEGREE C.
                                A 20 C. LA LECTURE EST DE 80H    */
 277    3                   IF TEMP$LOCAL>(80H+20) THEN TEMP$LOCAL=80H+20;
 279    3                   IF TEMP$LOCAL<(80H-60) THEN TEMP$LOCAL=80H-60;
 281    3                   TEMP$LOCAL=TEMP$LOCAL-(80H-60);
                            /* A CE POINT LA TEMPERATURE EN CELSIUS A
                               L'INTERIEUR EGALE 0 A 80 POUR -40 C. A +40 C.
                                                          */
                            /* GAIN A APPLIQUER EN FONCTION DE LA
                               TEMPERATURE AMBIANTE  */
 262    3                   TEMP=SHL(TEMP$LOCAL,1)+5;
 283    3                   TEMP=TEMP/10;
 284    3                   G=GAIN(TEMP);
                            /*  MESURE DU VOLTAGE DE REF. I.E. 0 DE L'APPAREIL */
 285    3                   CALL MESURE$REF;
 286    3                   LECTURE$V$AD=0;
 287    3               END;
 288    2           END CALIBRATION;
```

```
                $EJECT
                   /*                  ROUTINE D'INTERRUPTION
                                    --------------------------
                                                                      */
 289   1           INT$RADIOM: PROCEDURE INTERRUPT 7;
 290   2           DECLARE TEMP BYTE;
 291   2           DECLARE SOMME ADDRESS;
 292   2           DO;
 293   3           IF LECTURE$V$AD=1 THEN DO;
 295   4               DETECT$DEBUT$VEH=0;
 296   4               RETURN;
 297   4               END;
                   /* LECTURE TEMPERATURE DE LA ROUTE    */
 298   3           CALL MESURE$A$D(RADIOMETRE);
                   /*    COMPENSATION EN GAIN DU A LA TEMPERATURE AMBIANTE -
                         COMPENSATION DE -40 C. A 0 C. =( % DE LA TABLE *
                         T$ACTUEL)+ T$ACTUEL. COMPENSATION DE 0 C. A +40 C. =
                           % DE LA TABLE * T$ACTUEL      */
 299   3           IF TEMP$LOCAL>40 THEN DO;
 301   4               IF T$ACTUEL>=VREF THEN T$ACTUEL=(((T$ACTUEL-VREF)*G)/100)+
           -    VREF;
 303   4                                   ELSE T$ACTUEL=VREF-(((VREF-T$ACTUEL)*G)/
           -    100);
 304   4                 END;
 305   3             ELSE DO;
 306   4               IF T$ACTUEL>=VREF THEN DO;
 308   5                  TEMP=(((T$ACTUEL-VREF)*G)/100)+T$ACTUEL;
 309   5                  IF TEMP>T$ACTUEL THEN T$ACTUEL=TEMP;
 311   5                END;
 312   4              ELSE DO;
 313   5                  TEMP=T$ACTUEL-(((VREF-T$ACTUEL)*G)/100);
 314   5                  IF TEMP<T$ACTUEL THEN T$ACTUEL=TEMP;
 316   5                END;
 317   4             END;
                   /*   ENABLE DES INTERRUPT VENANT DU 422 ,MAIS DISABLE DES
                        INT 7.5 OU DES INT. VENANT DE L'HORLOGE A TOUTES
                        LES 10 M.SEC.     */
 318   3           TEMP=0DH;
 319   3           CALL S$MASK(TEMP);
 320   3           ENABLE;
                   /*    DETECTION FIN D'UN VEHICULE:?      */
 321   3           IF T$ACTUEL< SEUIL + TRESHOLD$SEUIL THEN DO;
 323   4               IF DETECT$DEBUT$VEH=1 THEN DO;
                          /*  ELIMINATION DU BRUIT < 60 M.SEC.  */
 325   5                  IF TA<6 THEN DO;
 327   6                      DETECT$DEBUT$VEH=0;
 328   6                      GOTO RETOURINT;
 329   6                      END;
 330   5                  IF (MAX-SEUIL)>SEUIL$SATURE THEN CAS$SATURE=1;
 332   5                                         ELSE CAS$SATURE=0;
 333   5                  IF TR>TF THEN TR=TF;
 335   5                           ELSE TF=TR;
 336   5                  IF SHR(TA,1) > TF THEN DO;
 338   6                      TB=TA-SHL(TF,1);
 339   6                      END;
 340   5                                   ELSE DO;
 341   6                      TB=0;
```

```
342   6                     TR=TA-TF;
343   6                     END;
                        /* CORRECTION DES TEMPS TR,TF ET TA DU AU TRESHOLD
      -    */
344   5                 TC=(MAX-(SEUIL+TRESHOLD$SEUIL))/TRESHOLD$SEUIL;
345   5                 TC=TF/TC;
346   5                 IF (TF MOD TC) > SHR(TC,1) THEN TC=TC+1;
348   5                 TF=TF+TC;
349   5                 TR=TR+TC;
350   5                 TA=TA+SHL(TC,1);
                        /* CALCUL DE LA LONGEUR ET VITESSE DU VEHICULE  */
351   5                 IF CAS$SATURE=0 THEN DO;
                            /* CAS NON SATURE */
353   6                     IF TB=0 THEN LONGEUR=H$AUTO;
355   6                             ELSE LONGEUR=((((TA-TB)*100)/(TA+TB))*H$AU
      -    TO+50)/100;
356   6                     VITESSE=(H$AUTO*68)/(TB+TR);
357   6                     END;
358   5                     ELSE DO;
                            /* CAS SATURE   */
359   6                     IF TB=0 THEN LONGEUR=H$CAMION;
361   6                             ELSE LONGEUR=(((TA+TB)/(TA-TB))*H$CAMION)
      -    +
                                                (((((((TA+TB)MOD(TA-TB))*100)
      -    /(TA-TB))
                                                   *H$CAMION)+50)/100);
      -
362   6                     VITESSE=((LONGEUR+H$CAMION)*68)/TA;
363   6                     END;
                        /* FORMATION DE L'INFORMATION DANS LE BUFFER  */
364   5                 CALL FORMATION$INFO;
365   5                 GOTO RETOURINT;
366   5               END;
367   4               ELSE DO;
                        /* CALCUL DU SEUIL BASE SUR MOY. DE 10 ECHANTILLONS
                                A TOUTES LES 200 M.SEC.      */
368   5               NB$MESURE=NB$MESURE+1;
369   5               IF NB$MESURE=20 THEN DO;
371   6                   NB$MESURE=0;
372   6                   IF T$ACTUEL<SEUIL THEN DO;
374   7                      IF SEUIL>TRESHOLD$NEGATIF AND T$ACTUEL<(SEUIL-TRESH
      -    OLD$NEGATIF)
                                THEN DO;
376   8                             TN=TN+1;
                                    /* SI APRES 10 SEC. LE SIGNAL EST TOUJOURS
      -     NEGATIF
                                       ALORS REAJUSTEMENT A CETTE VALEUR     *
      -    /
377   8                             IF TN>50 THEN DO;
379   9                              TN=0;
380   9                              DO K=0 TO 9;
381   10                                TEMP$AMB(K)=T$ACTUEL;
382   10                             END;
383   9                              SEUIL=T$ACTUEL;
384   9                            END;
385   8                           GOTO RETOURINT;
386   8                       END;
```

```
 387   7                    END;
 388   6                  TN=0;
 389   6                  IF J>=10 THEN J=0;
 391   6                  TEMP$AMB(J)=T$ACTUEL;
 392   6                  J=J+1;
 393   6                  SOMME=0;
 394   6                  DO K=0 TO 9;
 395   7                      SOMME=SOMME+TEMP$AMB(K);
 396   7                     END;
 397   6                  SEUIL=SOMME/10;
 398   6                 END;
 399   5               GOTO RETOURINT;
 400   5                 END;
 401   4             END;
                     /* PRESENSE D'UN VEHICULE SOUS DETECTEUR   */
 402   3             IF DETECT$DEBUT$VEH=0 THEN DO;
                         /* DONC DEBUT PRESENCE DU VEHICULE */
 404   4                 SEUIL$TB=0;
 405   4                 TF=0;
 406   4                 TA=0;
 407   4                 DETECT$DEBUT$VEH=1;
 408   4                 MAX=0;
 409   4                   END;
 410   3             TA=TA+1;
 411   3             IF T$ACTUEL>MAX THEN DO;
 413   4                 TF=0;
 414   4                 TR=TA;
 415   4                 MAX=T$ACTUEL;
 416   4                 SEUIL$TB=MAX-SHR(MAX-SEUIL,2);
 417   4                   END;
 418   3             IF T$ACTUEL < SEUIL$TB THEN TF=TF+1;
                     /* CAS D'ERREUR : TEMPS LIMITTE SOUS DETECTEUR = 20 SEC.
                        LE SEUIL EST REAJUSTE A CETTE NOUVELLE VALEUR     */
 420   3             IF DETECT$DEBUT$VEH=1 AND TA > 2000  THEN DO;
 422   4                 VITESSE=0;
 423   4                 LONGEUR=0;
 424   4                 DO K=0 TO 9;
 425   5                     TEMP$AMB(K)=T$ACTUEL;
 426   5                   END;
 427   4                 SEUIL=T$ACTUEL;
 428   4                 CALL FORMATION$INFO;
 429   4               END;
 430   3             RETOURINT: DISABLE;
 431   3                        TEMP=09H;
 432   3                        CALL S$MASK(TEMP);
 433   3                        RETURN;
 434   3             END;
 435   2         END INT$RADIOM;
```

```
                $EJECT
                    /*    TRANSMISSION A L'IMPRIMANTE OU INTERFACE RS-232C
                          ------------------------------------------------
                                                                        */
436   1           TRANS$232: PROCEDURE;
437   2           DECLARE (I,STATUS,ETAT$EQUIPEMENT) BYTE;
438   2           DO;
439   3           ETAT$EQUIPEMENT=INPUT(STATUS$232) AND 80H;
440   3           IF ETAT$EQUIPEMENT=0 THEN RETURN;
442   3           BUFFER$232(5)=(VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE + 1)
          -     AND 0FH)+'0';
443   3           BUFFER$232(4)=SHR((VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE
          -    + 1) AND 0F0H),4)+'0';
444   3           BUFFER$232(2)=(VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE) AND
          -     0FH)+'0';
445   3           BUFFER$232(1)=SHR((VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE)
          -     AND 0F0H),4)+'0';
446   3           BUFFER$232(7)=(VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE +3)/
          -    100)+'0';
447   3           BUFFER$232(8)=VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE + 3)
          -    MOD 100;
448   3           BUFFER$232(8)=(BUFFER$232(8) / 10 ) + '0';
449   3           BUFFER$232(9)=(VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE + 3)
          -     MOD 10)+ '0';
450   3           BUFFER$232(11)=(VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE+2)/
          -    10);
451   3           IF BUFFER$232(11) > 9 THEN BUFFER$232(11)=BUFFER$232(11)+'7';
453   3                                 ELSE BUFFER$232(11)=BUFFER$232(11)+'0';
454   3           BUFFER$232(12)=(VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE+2)
          -    MOD 10 )+ '0';
455   3           DO I=0 TO 14;
456   4               STATUS=0;
457   4               DO WHILE STATUS=0;
458   5                   STATUS=INPUT(STATUS$232) AND 1;
459   5                   ETAT$EQUIPEMENT=INPUT(STATUS$232) AND 80H;
460   5                   IF ETAT$EQUIPEMENT=0 THEN RETURN;
462   5                    END;
463   4               OUTPUT(DATA$232$OUT)=BUFFER$232(I);
464   4              END;
465   3           END;
466   2       END TRANS$232;
```

```
                $EJECT
                    /*      INSPECTION DU MESSAGE RECU ET DETECTION DE LA
                            ---------------------------------------------
                            REPONSE REQUISE
                            ---------------                              */
 467   1          INSPEC$REC$BUFFER: PROCEDURE;
 468   2          DECLARE (I,TOP,COMP) BYTE;
 469   2          DO;
 470   3          TOP=POINTEUR$REC -1;
 471   3          POINTEUR$REC=0;
 472   3          REC$COMPLETE=0;
 473   3          IF ERROR <> 0 THEN DO;
 475   4              ERROR=0;
 476   4              RETURN;
 477   4               END;
 478   3          IF REC$BUFFER(0)<> SOH THEN RETURN;
 480   3          IF REC$BUFFER(1) <> DETECT$ADD THEN RETURN;
 482   3          IF REC$BUFFER(2) <> ENQ THEN RETURN;
 484   3          IF REC$BUFFER(TOP) <> EOT THEN RETURN;
 486   3          IF REC$BUFFER(TOP-2) <> ETX THEN RETURN;
 488   3          LPC=0;
 489   3          DO I=0 TO (TOP - 2);
 490   4              LPC=LPC XOR REC$BUFFER(I);
 491   4              END;
 492   3          IF REC$BUFFER(TOP-1) <> LPC THEN RETURN;
                    /* QUEL MESSAGE A ETE RECU ?     */
 494   3          IF REC$BUFFER(3)='T' THEN DO;
 496   4              IF REC$BUFFER(4)='C' THEN DO;
 498   5                  MESSAGE=0;
 499   5                  RETURN;
 500   5                  END;
 501   4              IF REC$BUFFER(4)='P' THEN DO;
 503   5                  MESSAGE=1;
 504   5                  RETURN;
 505   5                  END;
 506   4              RETURN;
 507   4              END;
 508   3          IF REC$BUFFER(3)='D' THEN DO;
 510   4              IF REC$BUFFER(4)='C' THEN DO;
 512   5                  MESSAGE=2;
 513   5                  RETURN;
 514   5                   END;
 515   4              IF REC$BUFFER(4)='P' THEN DO;
 517   5                  MESSAGE=3;
 518   5                  RETURN;
 519   5                   END;
 520   4              RETURN;
 521   4              END;
 522   3          IF REC$BUFFER(3)='R' AND REC$BUFFER(4)='M' THEN DO;
 524   4              IF REC$BUFFER(5)='C' THEN DO;
 526   5                  MESSAGE=4;
 527   5                  RETURN;
 528   5                   END;
 529   4              IF REC$BUFFER(5)='P' THEN DO;
 531   5                  MESSAGE=5;
 532   5                  RETURN;
 533   5                   END;
```

```
534   4                RETURN;
535   4                 END;
536   3             IF REC$BUFFER(3)='Y' AND REC$BUFFER(4)='M' THEN DO;
538   4                 IF REC$BUFFER(5)='D' AND REC$BUFFER(6)='H' AND REC$BUFFER(
          -   7)='M' AND REC$BUFFER(8)='S' THEN DO;
540   5                     MESSAGE=6;
541   5                     RETURN;
542   5                      END;
543   4                 RETURN;
544   4                  END;
545   3             IF REC$BUFFER(3)='C' AND REC$BUFFER(4)='R' THEN DO;
547   4                 MESSAGE=7;
548   4                 RETURN;
549   4                   END;
550   3             IF REC$BUFFER(3)='Q' AND REC$BUFFER(4)='I' THEN DO;
552   4                 MESSAGE=8;
553   4                 RETURN;
554   4                   END;
555   3             IF REC$BUFFER(3)='Y' AND REC$BUFFER(6)='M' THEN DO;
557   4                 IF REC$BUFFER(9)='D' AND REC$BUFFER(12)='H' AND REC$BUFFER
          -   (15)='M' AND REC$BUFFER(18)='S' THEN DO;
559   5                     MESSAGE=9;
560   5                     RETURN;
561   5                      END;
562   4                 RETURN;
563   4                 END;
564   3             IF REC$BUFFER(3)='S' AND REC$BUFFER(4)='T' THEN DO;
566   4                 IF REC$BUFFER(5)='C' OR REC$BUFFER(5)='P' THEN DO;
568   5                     COMP=REC$BUFFER(5);
569   5                     DO I=3 TO TOP-5 BY 5;
570   6                         IF REC$BUFFER(I)<>'S' OR REC$BUFFER(I+1)<>'T' OR R
          -   EC$BUFFER(I+2)<>COMP THEN RETURN;
572   6                         IF REC$BUFFER(I+3) <'1' OR REC$BUFFER(I+3) >'5' TH
          -   EN RETURN;
574   6                         IF REC$BUFFER(I+4)<'1' OR REC$BUFFER(I+4) >'5' THE
          -   N RETURN;
576   6                           END;
577   5                     IF REC$BUFFER(5)='C' THEN MESSAGE=10;
579   5                          ELSE MESSAGE=11;
580   5                       END;
581   4                 END;
582   3             IF REC$BUFFER(3)='R' AND REC$BUFFER(4)='Q' AND REC$BUFFER(5)='
          -   I' THEN DO;
584   4                 MESSAGE=12;
585   4                 RETURN;
586   4                  END;
587   3             END;
588   2         END INSPEC$REC$BUFFER;
```

```
                 $EJECT
                   /$
                      LECTURE DU STATUS DU TRANSMETEUR I.E. READY BIT DU RS422
                      ---------------------------------------------------------
                -   /                                                          ------- $
589    1             TRANS$READY$422: PROCEDURE PUBLIC;
390    2             DECLARE STATUS BYTE;
591    2             DO;
592    3             STATUS=0;
593    3             DO WHILE STATUS=0;
594    4                 STATUS=INPUT(STATUS$422) AND 1;
595    4                   END;
596    3             END;
597    2         END TRANS$READY$422;
```

```
                $EJECT
                    /*
                       PROCEDURE POUR TRANSMETTRE UNE PARTIE D'UN MESSAGE
                       --------------------------------------------------
                        CONTENU DANS LE BUFFER TRANS$BUFFER              */
598    1           TRANS$BUFFER$MESS: PROCEDURE (FIN);
599    2           DECLARE (FIN,I) BYTE;
600    2           DO;
601    3              DO I=0 TO FIN;
602    4               CALL TRANS$READY$422;
603    4               OUTPUT(DATA$422$OUT)=TRANS$BUFFER(I);
604    4               LPC=LPC XOR TRANS$BUFFER(I);
605    4                END;
606    3           END;
607    2       END TRANS$BUFFER$MESS;
```

```
                $EJECT
                    /*
                       PROCEDURE POUR ATTENDRE UN TEMPS DETERMINE
                       ------------------------------------------
                        TEMPS=NB* 1 M.SEC.                                  */
608    1           TEMPS$MSEC: PROCEDURE (NB);
609    2           DECLARE (NB,I) BYTE;
610    2           DO;
611    3               DO I=0 TO NB;
612    4                   CALL TIME(10);
613    4                 END;
614    3            END;
615    2           END TEMPS$MSEC;
```

```
                $EJECT
                    /*
                       TRANSMETTRE UNE PARTIE D'UN MESSAGE ET
                       --------------------------------------
                       DE FAIRE LA TRANSFORMATION DE BINAIRE EN ASCII
                       ----------------------------------------------
                                                                     */
 616   1          TRANS$MESS$SUB: PROCEDURE (NOMBRE$B,EMPLACEMENT);
 617   2          DECLARE (TEMP,NOMBRE$B) ADDRESS;
 618   2          DECLARE EMPLACEMENT BYTE;
 619   2          DO;
 620   3          TRANS$BUFFER(EMPLACEMENT)=(NOMBRE$B/10000)+'0';
 621   3          TEMP=NOMBRE$B MOD 10000;
 622   3          TRANS$BUFFER(EMPLACEMENT + 1)=TEMP/1000 + '0';
 623   3          TEMP=TEMP MOD 1000;
 624   3          TRANS$BUFFER(EMPLACEMENT + 2)=TEMP/100 + '0';
 625   3          TEMP=TEMP MOD 100;
 626   3          TRANS$BUFFER(EMPLACEMENT + 3)=TEMP /10 + '0';
 627   3          TEMP=TEMP MOD 10;
 628   3          TRANS$BUFFER(EMPLACEMENT + 4)=TEMP + '0';
 629   3          CALL TRANS$BUFFER$MESS (EMPLACEMENT + 4);
 630   3          END;
 631   2      END TRANS$MESS$SUB;
```

```
                $EJECT
                    /*
                       TRANSMETTRE MESSAGE NO:0 OU 1;
                       TOTAL CUMULATIF OU PARTIEL DES VEHICULES
                       ---------------------------------------
                       DEPUIS LA REMISE A 0 DE LA MEMOIRE CUMULATIVE
                       OU PARTIEL                                    */
  632   1          TRANS$MESS$TOTAL$CP: PROCEDURE (CARACTERE,M$POINTEUR);
  633   2          DECLARE (CARACTERE,I) BYTE;
  634   2          DECLARE (SOMME,M$POINTEUR) ADDRESS;
  635   2          DECLARE (M BASED M$POINTEUR) (5) STRUCTURE (V(6) ADDRESS);
  636   2          DO;
  637   3          SOMME=0;
  638   3            DO I=0 TO 4;
  639   4              SOMME=SOMME+M(I).V(5);
  640   4               END;
  641   3          TRANS$BUFFER(0)='T';
  642   3          TRANS$BUFFER(1)=CARACTERE;
  643   3          CALL TRANS$MESS$SUB (SOMME,2);
  644   3          END;
  645   2      END TRANS$MESS$TOTAL$CP;
```

```
                $EJECT
                    /*
                       TRANSMETTRE LE MESSAGE 2 OU 3;
                       DETAIL DES COMPTES DES VEHICULES PAR CATEGORIES
                       -----------------------------------------------
                       DE LONGEUR ET DE VITESSE,RESULTATS CUMULATIF OU PARTIEL  */
646   1           TRANS$MESS$DETAIL$DCP: PROCEDURE (CARACTERE,M$POINTEUR);
647   2           DECLARE (TEMP,M$POINTEUR) ADDRESS;
648   2           DECLARE (I,J,CARACTERE) BYTE;
649   2           DECLARE (M BASED M$POINTEUR) (5) STRUCTURE (V(6) ADDRESS);
650   2           DO;
651   3           TRANS$BUFFER(0)='D';
652   3           TRANS$BUFFER(1)=CARACTERE;
653   3           CALL TRANS$BUFFER$MESS (1);
654   3           DO I=0 TO 4;
655   4               DO J=0 TO 4;
656   5                   TRANS$BUFFER(0)='L';
657   5                   TRANS$BUFFER(1)=I+'1';
658   5                   TRANS$BUFFER(2)='V';
659   5                   TRANS$BUFFER(3)=J+'1';
660   5                   TRANS$BUFFER(4)=SLASH;
661   5                   TEMP=M(I).V(J);
662   5                   CALL TRANS$MESS$SUB (TEMP,5);
663   5                    END;
664   4                END;
665   3           END;
666   2       END TRANS$MESS$DETAIL$DCP;
```

```
                $EJECT
                    /*
                      TRANSMETTRE LE MESSAGE NO. 4 OU 5
                       ET EXECUTER LA REMISE A 0 DE LA MEMOIRE CUMULATIVE
                       ----------------------------------------------
                       OU PARTIELLE
                       ------------                                    */
 667   1          RESET$MEMORY$CP: PROCEDURE (CARACTERE,M$POINTEUR);
 668   2          DECLARE (I,J,CARACTERE) BYTE;
 669   2          DECLARE M$POINTEUR ADDRESS;
 670   2          DECLARE (M BASED M$POINTEUR) (5) STRUCTURE (V(6) ADDRESS);
 671   2          DO;
 672   3              DO I=0 TO 4;
 673   4                  DO J=0 TO 5;
 674   5                      M(I).V(J)=0;
 675   5                      END;
 676   4                  END;
 677   3          TRANS$BUFFER(0)='R';
 678   3          TRANS$BUFFER(1)='M';
 679   3          TRANS$BUFFER(2)=CARACTERE;
 680   3          CALL TRANS$BUFFER$MESS (2);
 681   3          END;
 682   2      END RESET$MEMORY$CP;
```

```
                $EJECT
                    /*
                      TRANSMETTRE LE MESSAGE NO. 6 C.A.D.
                      LECTURE DE L'HORLOGE ET DU CALENDRIER INTERNE
                      ---------------------------------------------
                      , SYSTEME 24 HEURES          */
683   1           TRANS$MESS$CALENDAR: PROCEDURE;
                  /* ROUTINE POUR LIRE L'HORLOGE   */
684   2           READ$CLK: PROCEDURE ;
685   3           DECLARE (STATUS,I,J) BYTE;
686   3           DECLARE TEMP(5) BYTE;
687   3           DO;
688   4           STATUS=1;
689   4           DO WHILE STATUS;
690   5               TEMP(0)=INPUT(CLK$MONTH);
691   5               TEMP(1)=INPUT(CLK$DAY$MONTH);
692   5               TEMP(2)=INPUT(CLK$HOURS);
693   5               TEMP(3)=INPUT(CLK$MIN);
694   5               TEMP(4)=INPUT(CLK$SEC);
695   5               STATUS=INPUT(CLK$STATUS$BIT);
696   5               END;
                  /*    TRANS$BUFFER INDICE 0:MOIS,1:M(LSD),2:DAY,3:DAY(LSD),
                          ECT.. */
697   4           J=0;
698   4           DO I=4 TO 16 BY 3;
699   5               TRANS$BUFFER(I)=SHR((TEMP(J) AND 0F0H),4)+BCD$BASE;
700   5               TRANS$BUFFER(I+1)=(TEMP(J) AND 0FH)+BCD$BASE;
701   5               J=J+1;
702   5             END;
703   4           END;
704   3       END READ$CLK;
705   2           DO;
706   3           TRANS$BUFFER(0)='Y';
707   3           TRANS$BUFFER(1)=YEAR(0);
708   3           TRANS$BUFFER(2)=YEAR(1);
709   3           TRANS$BUFFER(3)='M';
710   3           TRANS$BUFFER(6)='D';
711   3           TRANS$BUFFER(9)='H';
712   3           TRANS$BUFFER(12)='M';
713   3           TRANS$BUFFER(15)='S';
714   3           CALL READ$CLK;
715   3           CALL TRANS$BUFFER$MESS(17);
716   3           END;
717   2       END TRANS$MESS$CALENDAR;
```

```
                $EJECT
                    /*
                       TRANSMETTRE LE MESSAGE NO. 7;
                       L'ETAT DE LA ROUTE
                       ------------------
                       EST DETERMINE A TOUTES LES DEMI-HEURES ET CUMULE POUR
                       24 HEURES. L'ETAT DE LA ROUTE PEUT ETRE : SEC (S),
                       MOUILLE (M),GLACE (G) OU INCONNU (?)                  */
718   1             TRANS$MESS$CR: PROCEDURE;
719   2             DECLARE (I,J) BYTE;
720   2             DO;
721   3             TRANS$BUFFER(0)='C';
722   3             TRANS$BUFFER(1)='R';
723   3             J=1;
724   3             DO I=POINTEUR$ETAT$ROUTE TO 47;
725   4                 J=J+1;
726   4                 TRANS$BUFFER(J)=ETAT$ROUTE(I);
727   4                 END;
728   3             IF POINTEUR$ETAT$ROUTE <> 0 THEN DO I=0 TO POINTEUR$ETAT$ROUTE
          -    - 1;
730   4                     J=J+1;
731   4                     TRANS$BUFFER(J)=ETAT$ROUTE(I);
732   4                   END;
733   3             CALL TRANS$BUFFER$MESS (J);
734   3             END;
735   2         END TRANS$MESS$CR;
```

```
                $EJECT
                    /*
                       TRANSMETTRE LE MESSAGE NO. 8 :
                       L'INFORMATION CONTENUE DANS LA QUEUE D'INFORMATION
                       -------------------------------------------------
                       EST ENVOYE A L'ORDINATEUR          */
 736    1           TRANS$QUEUE$INFO: PROCEDURE;
 737    2           DECLARE FIN BYTE;
                    /*       ROUTINE POUR TRANSMETTRE L'INFORMATION CONTENUE
                             DANS LA QUEUE */
 738    2           TRANS$QUEUE: PROCEDURE (DEBUT,FIN);
 739    3           DECLARE (DEBUT,FIN,I) BYTE;
 740    3           DO;
 741    4           DO I=DEBUT TO FIN-1 BY 6;
 742    5               TRANS$BUFFER(0)=QUEUE$INFO(I);
 743    5               TRANS$BUFFER(1)=QUEUE$INFO(I+1);
 744    5               TRANS$BUFFER(2)=':';
 745    5               TRANS$BUFFER(3)=QUEUE$INFO(I+2);
 746    5               TRANS$BUFFER(4)=QUEUE$INFO(I+3);
 747    5               TRANS$BUFFER(5)=':';
 748    5               TRANS$BUFFER(6)=QUEUE$INFO(I+4);
 749    5               TRANS$BUFFER(7)=QUEUE$INFO(I+5);
 750    5               TRANS$BUFFER(8)=SLASH;
 751    5               CALL TRANS$BUFFER$MESS (8);
 752    5               END;
 753    4           END;
 754    3       END TRANS$QUEUE;
 755    2           DO;
 756    3           IF POINTEUR$LECTURE$DEBUT$QUEUE=POINTEUR$LECTURE$FIN$QUEUE THE
          -    N POINTEUR$LECTURE$FIN$QUEUE=POINTEUR$ECRITURE$QUEUE;
 758    3           TRANS$BUFFER(0)='0';
 759    3           TRANS$BUFFER(1)='I';
 760    3           CALL TRANS$BUFFER$MESS (1);
 761    3           IF POINTEUR$LECTURE$DEBUT$QUEUE=POINTEUR$LECTURE$FIN$QUEUE THE
          -    N RETURN;
 763    3           IF POINTEUR$LECTURE$DEBUT$QUEUE<POINTEUR$LECTURE$FIN$QUEUE THE
          -    N  FIN=POINTEUR$LECTURE$FIN$QUEUE;
 765    3                              ELSE  FIN=POINTEUR$MAX$QUEUE;
 766    3           CALL TRANS$QUEUE (POINTEUR$LECTURE$DEBUT$QUEUE,FIN);
 767    3           IF POINTEUR$LECTURE$DEBUT$QUEUE > POINTEUR$LECTURE$FIN$QUEUE T
          -    HEN CALL TRANS$QUEUE (0,POINTEUR$LECTURE$FIN$QUEUE);
 769    3           END;
 770    2       END TRANS$QUEUE$INFO;
```

```
                $EJECT
                    /*    ROUTINE POUR PROGRAMMER I.E. ECRIRE L'HORLOGE
                          ---------------------------------------------      */
 771    1           WRITE$CLK: PROCEDURE;
 772    2           DECLARE (I,J,TEMP1,TEMP2) BYTE;
 773    2           DECLARE TEMP(5) BYTE;
 774    2           DO;
 775    3           YEAR(0)=REC$BUFFER(4);
 776    3           YEAR(1)=REC$BUFFER(5);
 777    3           J=4;
 778    3           DO I=0 TO 4;
 779    4               J=J+3;
 780    4               TEMP1=REC$BUFFER(J)-BCD$BASE;
 781    4               TEMP1=SHL(TEMP1,4);
 782    4               TEMP2=REC$BUFFER(J+1)-BCD$BASE;
 783    4               TEMP(I)=TEMP1 OR TEMP2;
 784    4              END;
 785    3           OUTPUT(CLK$MONTH)=TEMP(0);
 786    3           OUTPUT(CLK$DAY$MONTH)=TEMP(1);
 787    3           OUTPUT(CLK$HOURS)=TEMP(2);
 788    3           OUTPUT(CLK$MIN)=TEMP(3);
 789    3           OUTPUT(CLK$SEC)=TEMP(4);
 790    3           END;
 791    2       END WRITE$CLK;
```

```
                $EJECT
                    /*
                      TRANSMETTRE LE MESSAGE NO. 9 ,
                      ET FAIRE LA REMISE A DATE DE L'HORLOGE ET DU CALENDRIER
                      ------------------------------------------------------
                      INTERNE.
                      ----------
                      LE SENSEUR REPOND PAR LA DATE ET L'HEURE QUE L'ORDINATEUR
                      LUI A ENVOYEES                                          */
  792   1           REMISE$DATE$CALENDAR: PROCEDURE;
  793   2           DECLARE I BYTE;
  794   2           DO;
  795   3           CALL WRITE$CLK;
  796   3           DO I=3 TO 20;
  797   4               CALL TRANS$READY$422;
  798   4               OUTPUT(DATA$422$OUT)=REC$BUFFER(I);
  799   4               LPC=LPC XOR REC$BUFFER(I);
  800   4               END;
  801   3           END;
  802   2       END REMISE$DATE$CALENDAR;
```

```
                $EJECT
                    /*
                      TRANSMETTRE LE MESSAGE 10 OU 11:
                      SOUS-TOTAUX CUMULATIFS OU PARTIELS PAR CATEGORIES
                      ------------------------------------------------
                      DE LONGEUR OU REGROUPEMENT DE LONGEURS
                      (REGROUPEMENT MAXIMUM DE 2 CATEGORIES A LA FOIS )     */
B03   1           TRANS$MESS$SOUS$TOTAUX: PROCEDURE (CARACTERE,M$POINTEUR);
B04   2           DECLARE (CARACTERE,I) BYTE;
B05   2           DECLARE (M$POINTEUR,SOMME) ADDRESS;
B06   2           DECLARE (M BASED M$POINTEUR) (5) STRUCTURE (V(6) ADDRESS);
B07   2           DO;
B08   3           I=3;
B09   3           DO WHILE REC$BUFFER(I) <> ETX;
B10   4               I=I+3;
B11   4               SOMME=M(REC$BUFFER(I)-'1').V(5);
B12   4               IF REC$BUFFER(I)<>REC$BUFFER(I+1) THEN SOMME=SOMME + M(REC
          $BUFFER(I+1)-'1').V(5);
B14   4               TRANS$BUFFER(0)='S';
B15   4               TRANS$BUFFER(1)='T';
B16   4               TRANS$BUFFER(2)=CARACTERE;
B17   4               TRANS$BUFFER(3)=REC$BUFFER(I);
B18   4               TRANS$BUFFER(4)=REC$BUFFER(I+1);
B19   4               TRANS$BUFFER(5)=SLASH;
B20   4               CALL TRANS$MESS$SUB (SOMME,6);
B21   4               I=I+2;
B22   4               END;
B23   3           END;
B24   2       END TRANS$MESS$SOUS$TOTAUX;
```

```
                $EJECT
                    /*
                      TRANSMETTRE LE MESSAGE NO. 12 ,
                      ET EXECUTER LA REMISE A 0 DE LA MEMOIRE DE QUEUE DE
                      ---------------------------------------------------
                      L'INFORMATION
                      -------------                                  */
 825   1          RESET$QUEUE$I: PROCEDURE;
 826   2          DO;
 827   3          POINTEUR$LECTURE$DEBUT$QUEUE=POINTEUR$LECTURE$FIN$QUEUE;
 828   3          TRANS$BUFFER(0)='R';
 829   3          TRANS$BUFFER(1)='Q';
 830   3          TRANS$BUFFER(2)='I';
 831   3          CALL TRANS$BUFFER$MESS (2);
 832   3          END;
 833   2      END RESET$QUEUE$I;
```

```
                $EJECT
                    /*
                      REPONDRE ET EXECUTER UNE COMMANDE VALIDE
                      ----------------------------------------    */
 834   1          TRANSMISSION: PROCEDURE;
 835   2          DECLARE BD BYTE;
 836   2          DO;
 837   3          OUTPUT(ADD$ENABLE$422)=ENTRANS$422;
 838   3          LPC=0;
 839   3          TRANS$BUFFER(0)=SOH;
 840   3          TRANS$BUFFER(1)=DETECT$ADD;
 841   3          TRANS$BUFFER(2)=STX;
 842   3          CALL TRANS$BUFFER$MESS (2);
 843   3          DO CASE MESSAGE;
 844   4              CALL TRANS$MESS$TOTAL$CP ('C',.MATRICE$CUMUL(0).V);
 845   4              CALL TRANS$MESS$TOTAL$CP ('P',.MATRICE$INTER(0).V);
 846   4              CALL TRANS$MESS$DETAIL$DCP ('C',.MATRICE$CUMUL(0).V);
 847   4              CALL TRANS$MESS$DETAIL$DCP ('P',.MATRICE$INTER(0).V);
 848   4              CALL RESET$MEMORY$CP ('C',.MATRICE$CUMUL(0).V);
 849   4              CALL RESET$MEMORY$CP ('P',.MATRICE$INTER(0).V);
 850   4              CALL TRANS$MESS$CALENDAR;
 851   4              CALL TRANS$MESS$CR;
 852   4              CALL TRANS$QUEUE$INFO;
 853   4              CALL REMISE$DATE$CALENDAR;
 854   4              CALL TRANS$MESS$SOUS$TOTAUX ('C',.MATRICE$CUMUL(0).V);
 855   4              CALL TRANS$MESS$SOUS$TOTAUX ('P',.MATRICE$INTER(0).V);
 856   4              CALL RESET$QUEUE$I;
 857   4               END;
 858   3          TRANS$BUFFER(0)=ETX;
 859   3          CALL TRANS$BUFFER$MESS (0);
 860   3          TRANS$BUFFER(0)=LPC;
 861   3          TRANS$BUFFER(1)=EOT;
 862   3          CALL TRANS$BUFFER$MESS (1);
 863   3          CALL TRANS$READY$422;
                  /*  ATTENDRE QUE LE DERNIER BYTE SOIT ENVOYE AVANT DE
                      METTRE DISABLE LE TRANSMETTEUR DU 422   */
 864   3          BD=BAUD$RATE$422$232 AND 70H;
 865   3          BD=SHR(BD,4);
 866   3          DO CASE BD;
 867   4              CALL TEMPS$MSEC (90);
 868   4              CALL TEMPS$MSEC (66);
 869   4              CALL TEMPS$MSEC (33);
 870   4              CALL TEMPS$MSEC (8);
 871   4              CALL TEMPS$MSEC (5);
 872   4              CALL TEMPS$MSEC (4);
 873   4              CALL TEMPS$MSEC (2);
 874   4              CALL TEMPS$MSEC (1);
 875   4            END;
 876   3          OUTPUT(ADD$ENABLE$422)=DISTRANS$422;
 877   3          END;
 878   2      END TRANSMISSION;
```

```
                $EJECT
                    /*
                        DEBUT PROGRAMME PRINCIPAL
                        -------------------------

 879   1                                                          */
                    DISABLE;
 880   1                CALL INITIALISATION;
                          /*   DELAIS DE MISE EN MARCHE: 5 MIN.
                               L'APPAREIL N'EST PAS OPERATIONNEL DURANT LES 5
                               PREMIERES MIN. DE MISE EN MARCHE
 881   1                DO J=1 TO 60;                                 */
 882   2                   DO I=1 TO 200;
 883   3                      CALL TIME(250);
 884   3                   END;
 885   2                END;
 886   1                CALL CALIBRATION;
                          /*    SET INTERRUPT MASK : SIM AVEC INT. 7.5 ET 6.5 ENABLE  */
 887   1                TEMP=19H;
 888   1                CALL S$MASK (TEMP);
 889   1                ENABLE;
                          /*   DEBUT DE LA BOUCLE
                          /*        CLASSER LE VEHICULE DANS LES MATRICES SI REQUIS    */
 890   1           BOUCLE: IF POINTEUR$ECRITURE$VEHICULE<>POINTEUR$LECTURE$VEHICULE T
               -    HEN DO;
 892   2                   IF VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE+3) >70 THEN  S
               -    PEED=4;
 894   2                   ELSE DO;
 895   3                      IF VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE+3) >40 T
               -    HEN SPEED=3;
 897   3                      ELSE DO;
 898   4                         IF VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE+3) >
               -    20 THEN SPEED=2;
 900   4                         ELSE DO;
 901   5                            IF VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICUL
               -    E+3) >10 THEN SPEED=1;
 903   5                            ELSE SPEED=0;
 904   5                         END;
 905   4                      END;
 906   3                   END;
 907   2                IF VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE+2) >40 THEN L=
               -    4;
 909   2                ELSE DO;
 910   3                   IF VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE+2) >28 T
               -    HEN L=3;
 912   3                   ELSE DO;
 913   4                      IF VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICULE+2) >
               -    18 THEN L=2;
 915   4                      ELSE DO;
 916   5                         IF VEHICULE$DETECTE(POINTEUR$LECTURE$VEHICUL
               -    E+2) >14 THEN L=1;
 918   5                         ELSE L=0;
 919   5                      END;
 920   4                   END;
 921   3                END;
 922   2             MATRICE$CUMUL(L).V(SPEED)=MATRICE$CUMUL(L).V(SPEED) + 1;
 923   2             MATRICE$INTER(L).V(SPEED)=MATRICE$INTER(L).V(SPEED) + 1;
 924   2             MATRICE$CUMUL(L).V(5)=MATRICE$CUMUL(L).V(5) + 1;
```

```
 925   2            MATRICE$INTER(L).V(5)=MATRICE$INTER(L).V(5) + 1;
                    /*   TRANSMETTRE LE MESSAGE POUR CE VEHICULE A L'IMPRIMANTE
                         I.E. SORTIE RS-232C        */
 926   2            CALL TRANS$232;
                    /*  PLACER LE VEHICULE DANS LA QUEUE D'INFORMATION        */
 927   2            QUEUE$INFO(POINTEUR$ECRITURE$QUEUE)=BUFFER$232(1);
 928   2            QUEUE$INFO(POINTEUR$ECRITURE$QUEUE+1)=BUFFER$232(2);
 929   2            QUEUE$INFO(POINTEUR$ECRITURE$QUEUE+2)=BUFFER$232(4);
 930   2            QUEUE$INFO(POINTEUR$ECRITURE$QUEUE+3)=BUFFER$232(5);
 931   2            QUEUE$INFO(POINTEUR$ECRITURE$QUEUE+4)=L+'1';
 932   2            QUEUE$INFO(POINTEUR$ECRITURE$QUEUE+5)=SPEED+ '1';
 933   2            POINTEUR$ECRITURE$QUEUE=POINTEUR$ECRITURE$QUEUE + 6;
 934   2            IF POINTEUR$ECRITURE$QUEUE>=POINTEUR$MAX$QUEUE THEN POINTEUR
       -    $ECRITURE$QUEUE=0;
                    /*   UP-DATE DU POINTEUR DE LECTURE DES VEHICULES      */
 936   2            POINTEUR$LECTURE$VEHICULE=POINTEUR$LECTURE$VEHICULE+4;
 937   2            IF POINTEUR$LECTURE$VEHICULE>=POINTEUR$MAX$VEHICULE$DETECTE
       -    THEN POINTEUR$LECTURE$VEHICULE=0;
 939   2          END;
                  /*  RECEPTION D'UN MESSAGE COMPLET ?.
                      SI OUI EXECUTER LA COMMANDE ET REPONDRE A CELLE-CI       */
       -    /
 940   1          IF REC$COMPLETE<>0 THEN DO;
 942   2              MESSAGE=255;
 943   2              CALL INSPEC$REC$BUFFER;
 944   2              IF MESSAGE<>255 THEN CALL TRANSMISSION;
 946   2              OUTPUT(COMM$CONT$422)=COMM$BYTE$RESET$422;
 947   2              OUTPUT(COMM$CONT$422)=COMM$BYTE$422;
 948   2              REC$PERMISSION=0FFH;
 949   2              END;
                  /*      L'ETAT DE LA ROUTE DOIT-ETRE CUMULLE
                          POUR LES DERNIERES 24 HEURES,A TOUTES LES DEMI-HEURES
                          (BIT 4:MIN , BIT 5:HEURE)
                                                          */
 950   1          TEMP=INPUT(CLK$INTERRUPT$STATUS);
 951   1          IF TEMP<>0 THEN DO;
 953   2              MIN=MIN+1;
 954   2              IF MIN>=5 OR (TEMP AND 10H)<>0 THEN DO;
 956   3                  T$MIN=T$MIN+1;
 957   3                  CALL CALIBRATION;
 958   3                  IF SEUIL<VREF THEN ETAT=0;
 960   3                                ELSE ETAT=SEUIL-VREF;
                         /* MEMORISATION DE L'ETAT DE LA ROUTE LE PLUS
                            DANGEREUX   */
 961   3                  IF ETAT>ETAT$R THEN ETAT$R=ETAT;
 963   3                  IF (TEMP AND 10H)<>0 OR T$MIN>=6  THEN DO;
 965   4                      ETAT=ETAT$R;
 966   4                      ETAT$R=0;
 967   4                      T$MIN=0;
                             /* UP-DATE DE L'ETAT DE LA ROUTE     */
 968   4                      IF ETAT>ETAT$MOUILLE THEN ETAT$ROUTE(POINTEUR$ETAT
       -    $ROUTE)='6';
 970   4                      IF ETAT>ETAT$SEC AND ETAT<=ETAT$MOUILLE
                                        THEN ETAT$ROUTE(POINTEUR$ETAT$ROUTE
       -    )='M';
 972   4                      IF ETAT<=ETAT$SEC THEN  ETAT$ROUTE(POINTEUR$ETAT$R
       -    OUTE)='S';
```

```
 974   4                        IF POINTEUR$ETAT$ROUTE>=47 THEN POINTEUR$ETAT$ROUT
             -   E=0;
 976   4                            ELSE POINTEUR$ETAT$ROUTE=POINTEUR$ETAT$ROUTE +
             -   1;
 977   4                    END;
 978   3                 END;
 979   2            END;
                   /*
                        FIN DE LA BOUCLE
                       ----------------------
                                                      */
 980   1            GOTO BOUCLE;
 981   1      END SENSEUR$VEHICULE;
              /*************************************************************************
             -  ***************************************************************/
```

MODULE INFORMATION:

```
     CODE AREA SIZE     = 1757H   5975D
     VARIABLE AREA SIZE = 0349H    841D
     MAXIMUM STACK SIZE = 000EH     14D
     1240 LINES READ
     0 PROGRAM ERRORS
```

END OF PL/M-80 COMPILATION